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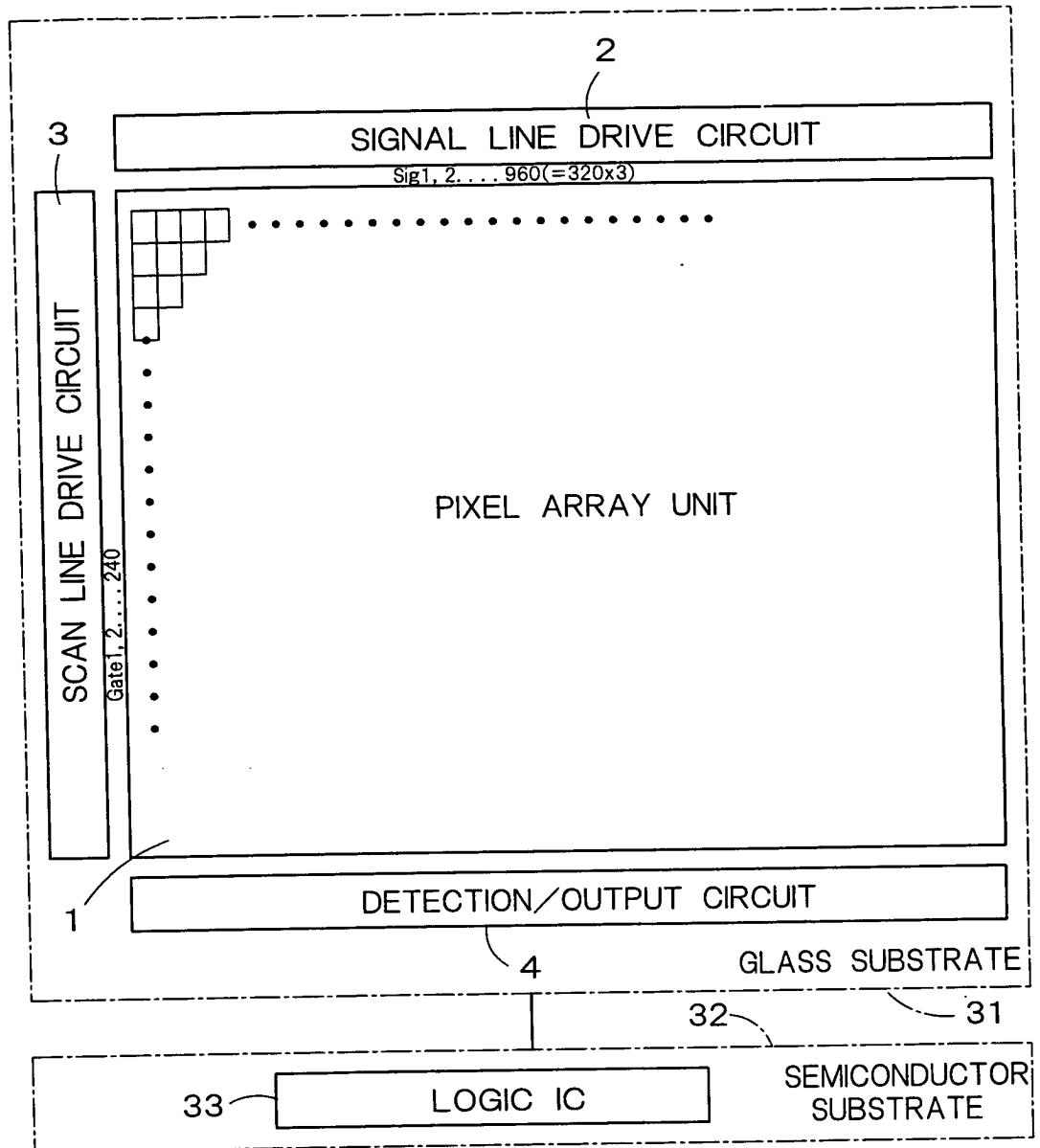


FIG. 1

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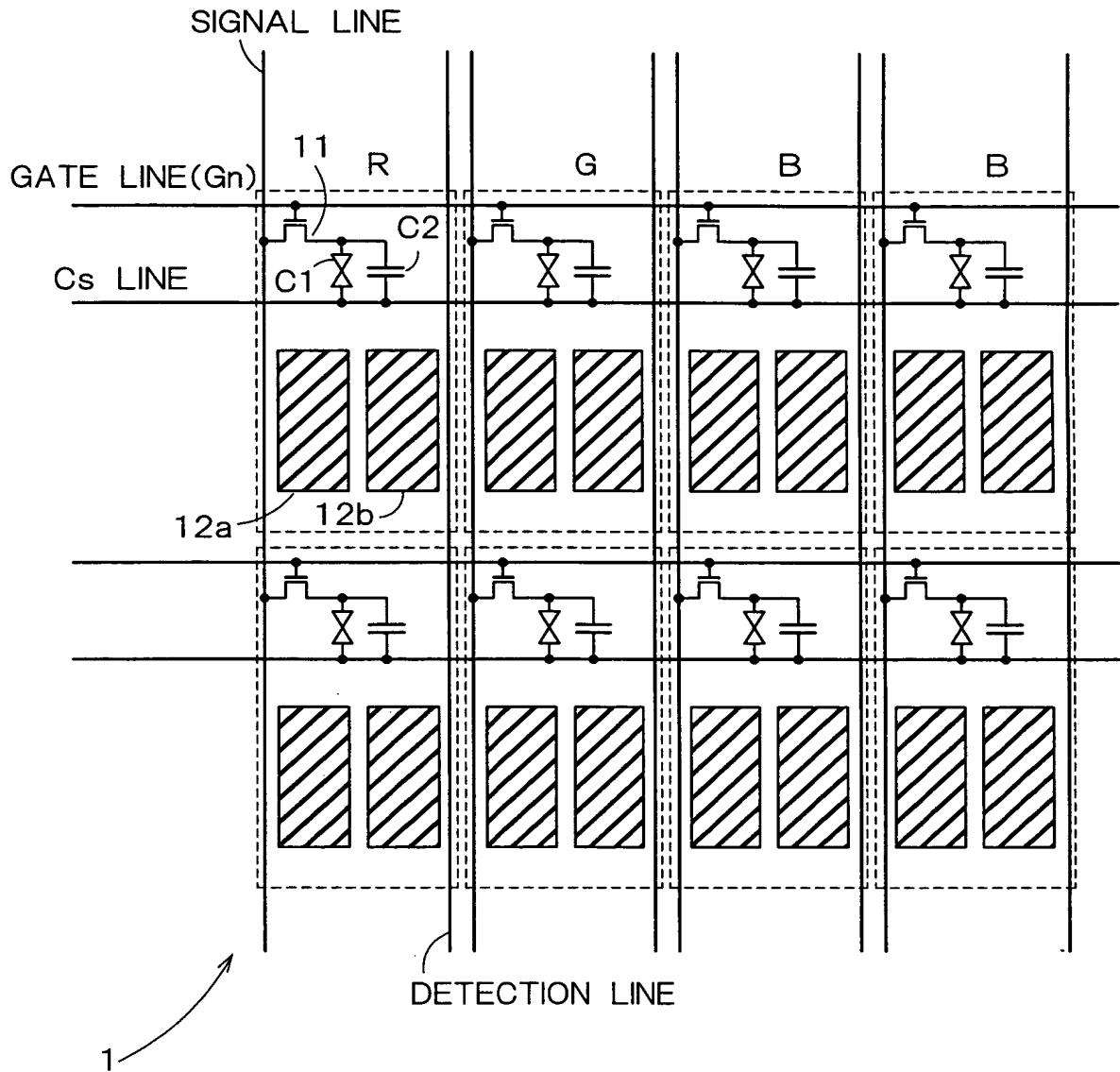


FIG. 2

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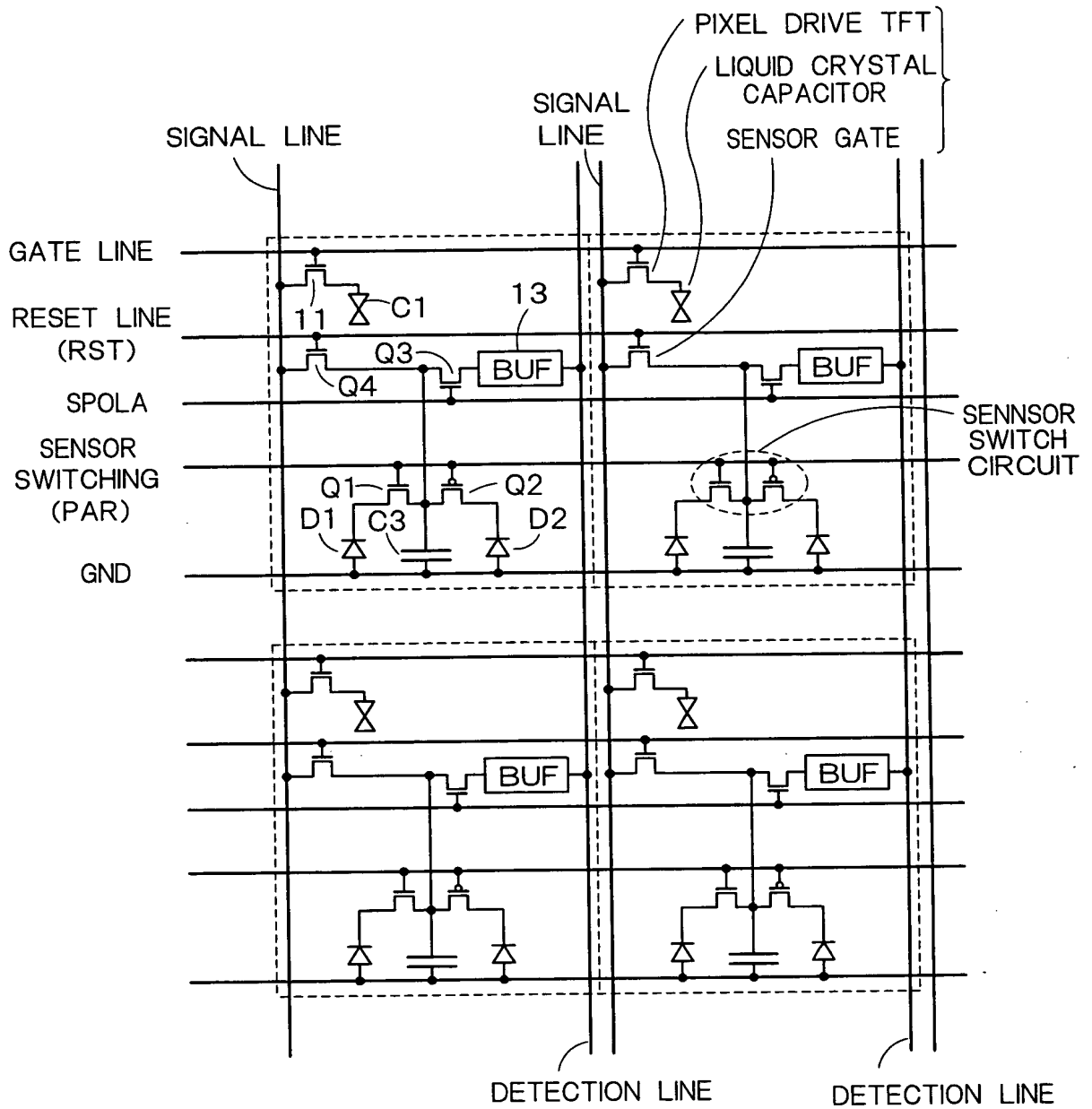


FIG. 3

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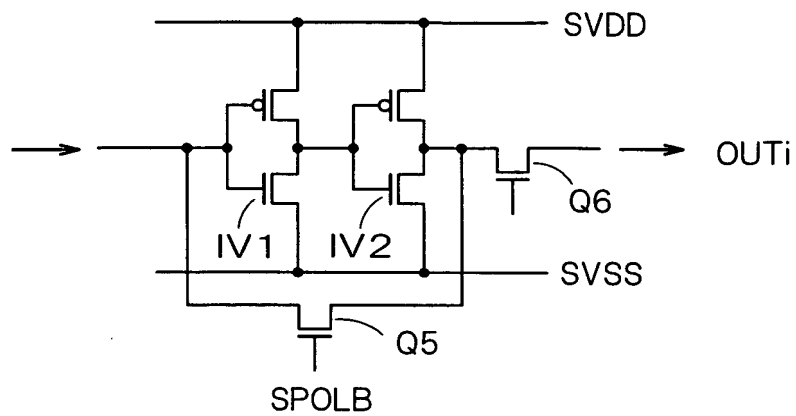


FIG. 4

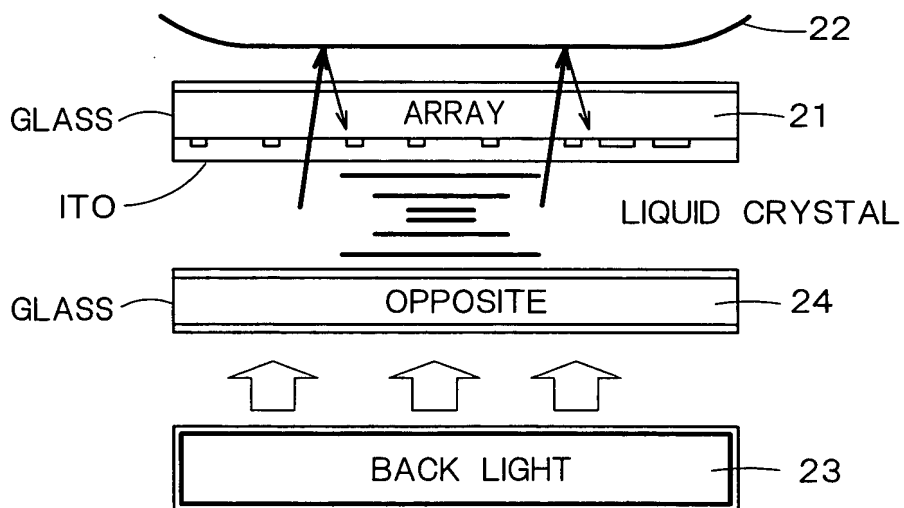


FIG. 5

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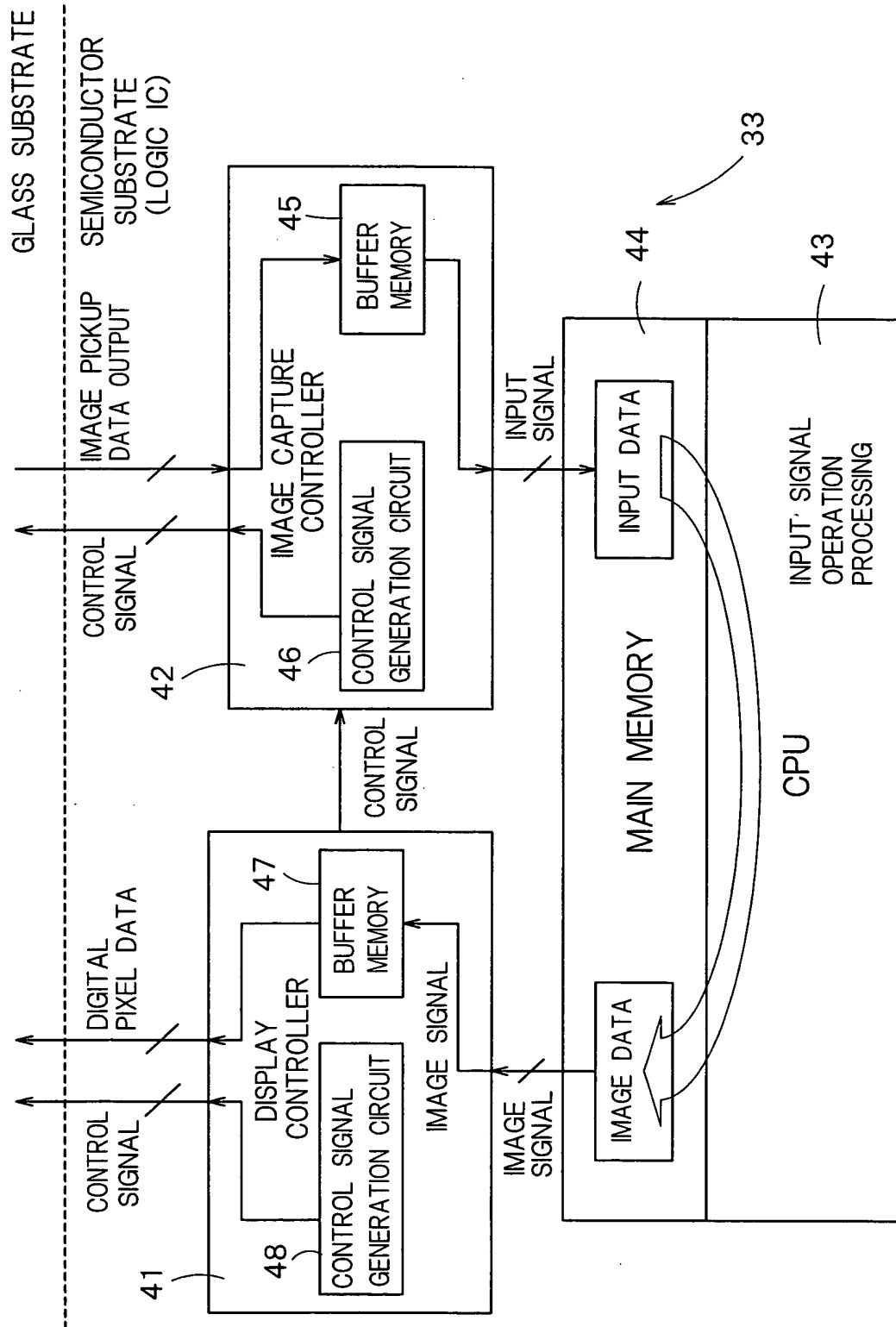


FIG. 6

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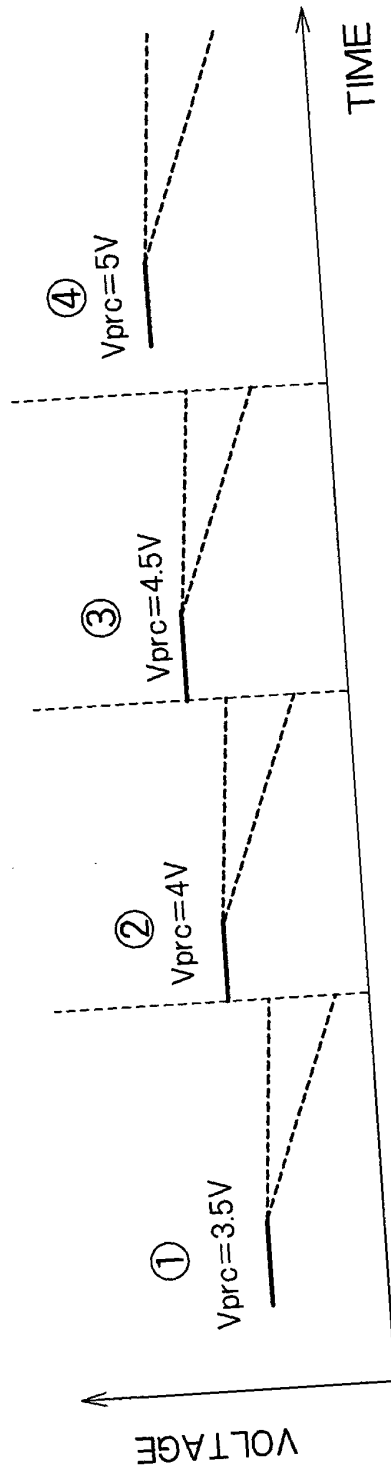


FIG. 7

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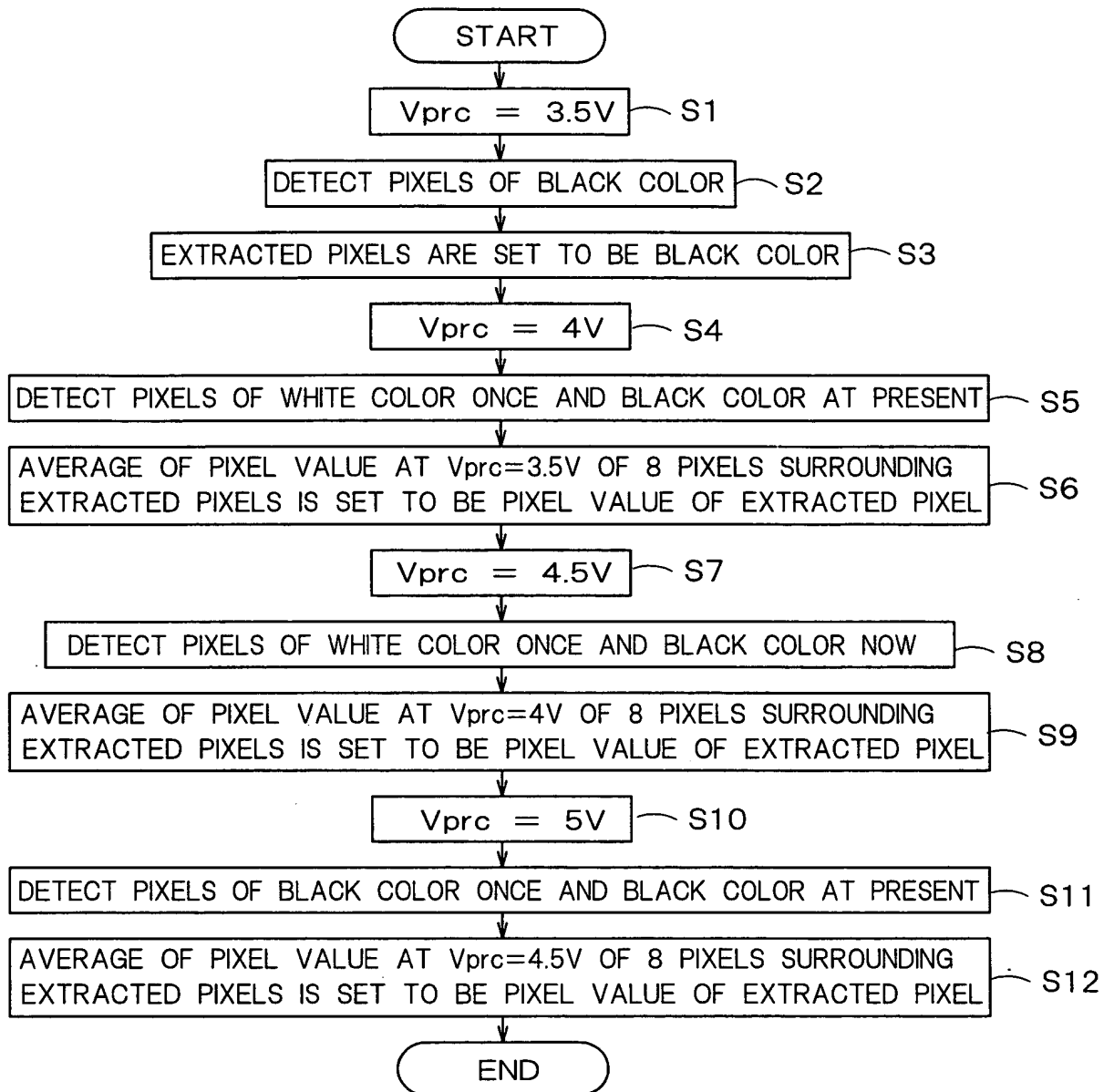


FIG. 8

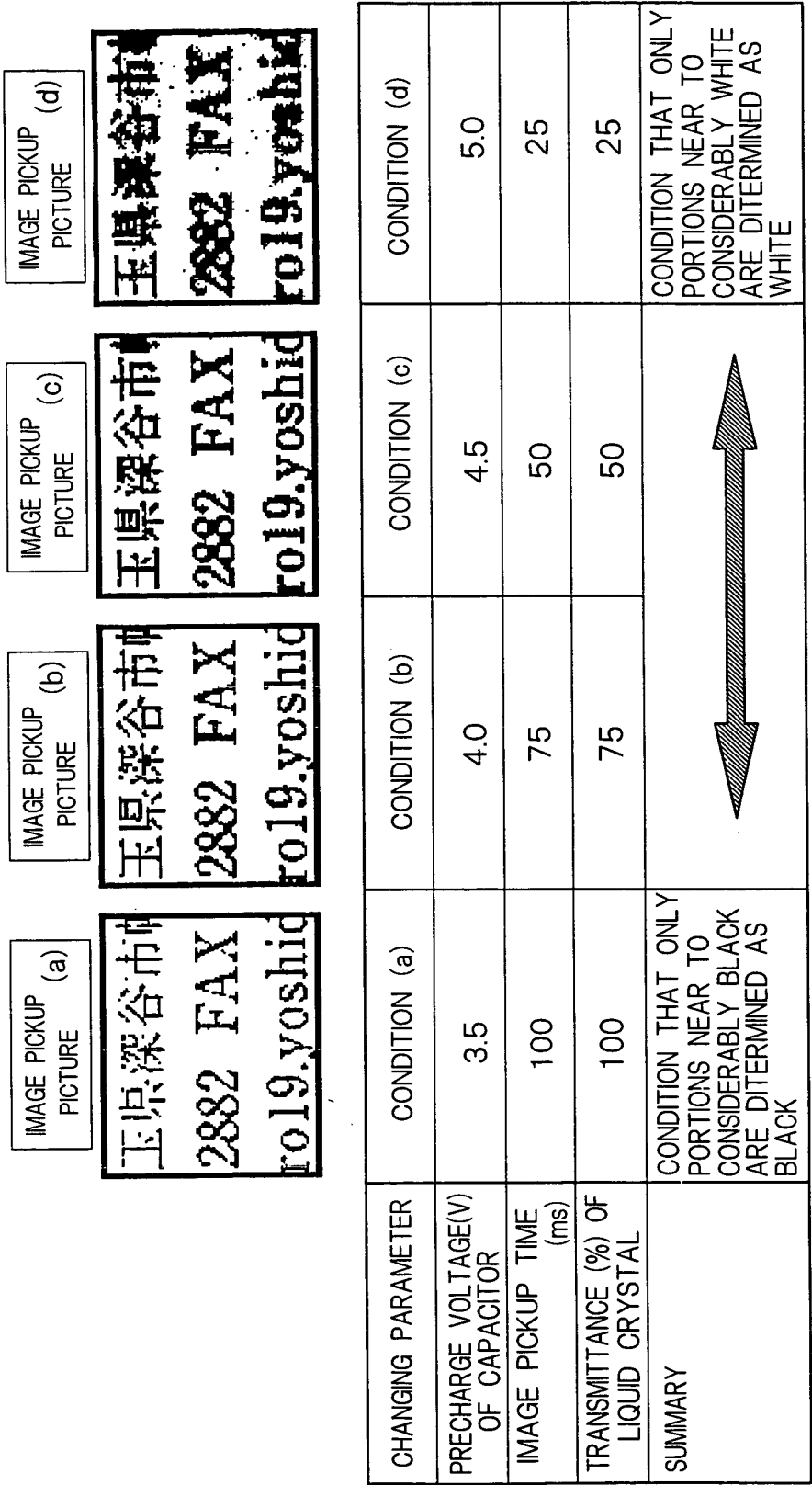


FIG. 9



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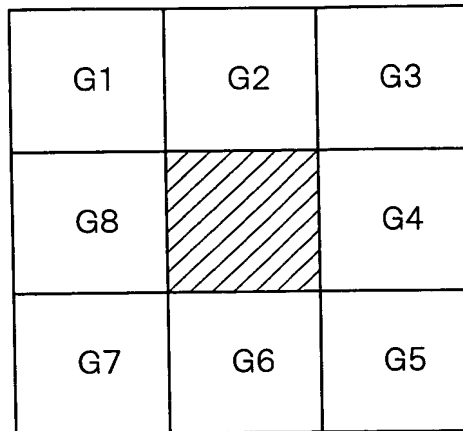


FIG. 10

玉泉深谷市  
2882 FAX  
rol9.yoshic

FIG. 11

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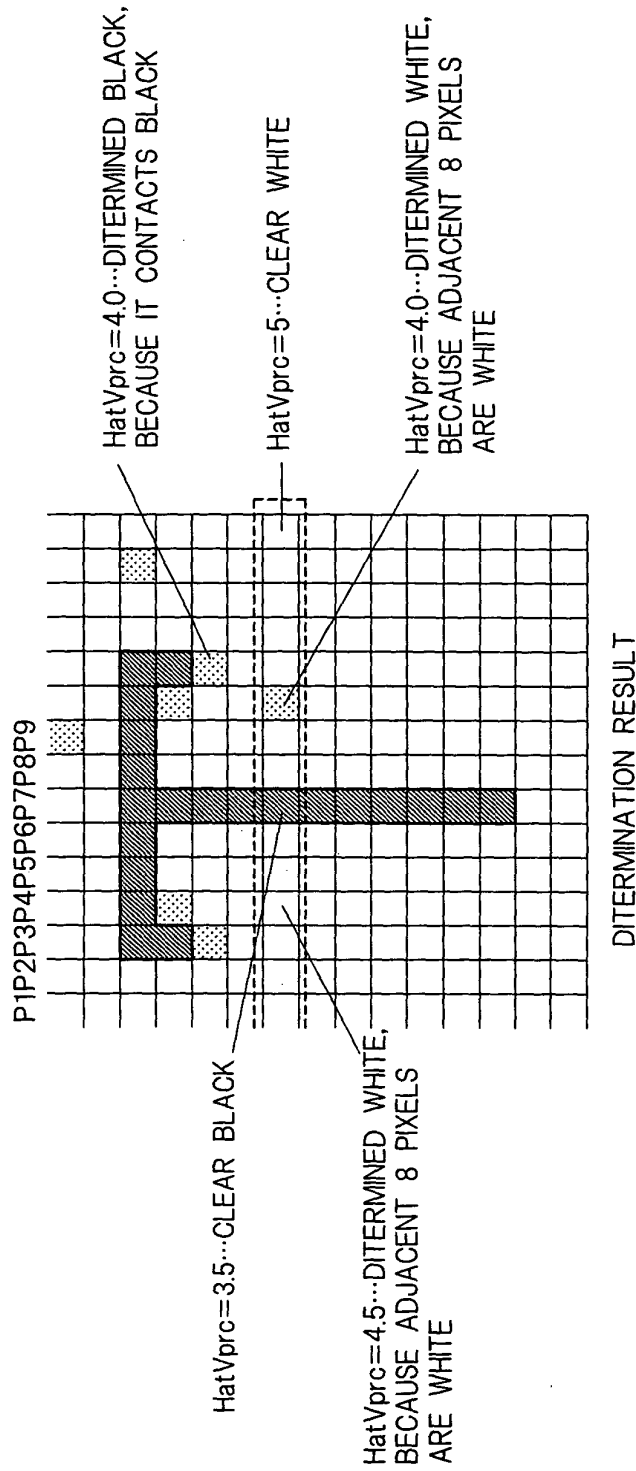


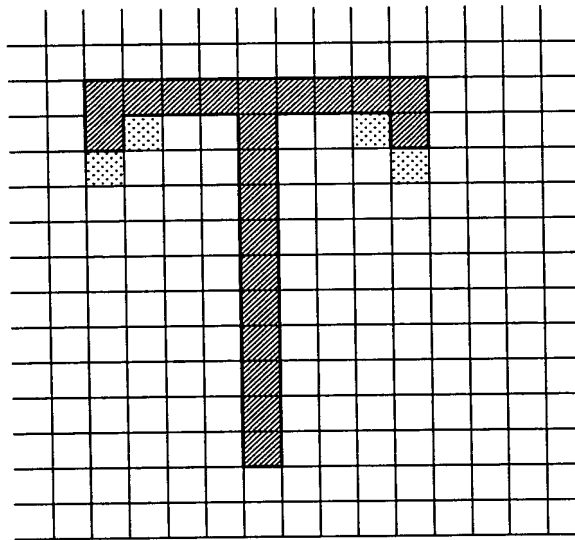
FIG. 12

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	Vprc(V)	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15
(a)	3.5	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
(b)	4.0	L	L	L	L	L	L	H	L	L	H	L	L	L	L	L
(c)	4.5	L	L	L	H	L	L	H	L	L	H	L	L	L	L	L
(d)	5.0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

FIG. 13

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REPRODUCED IMAGE ON DISPLAY DEVICE

FIG. 14

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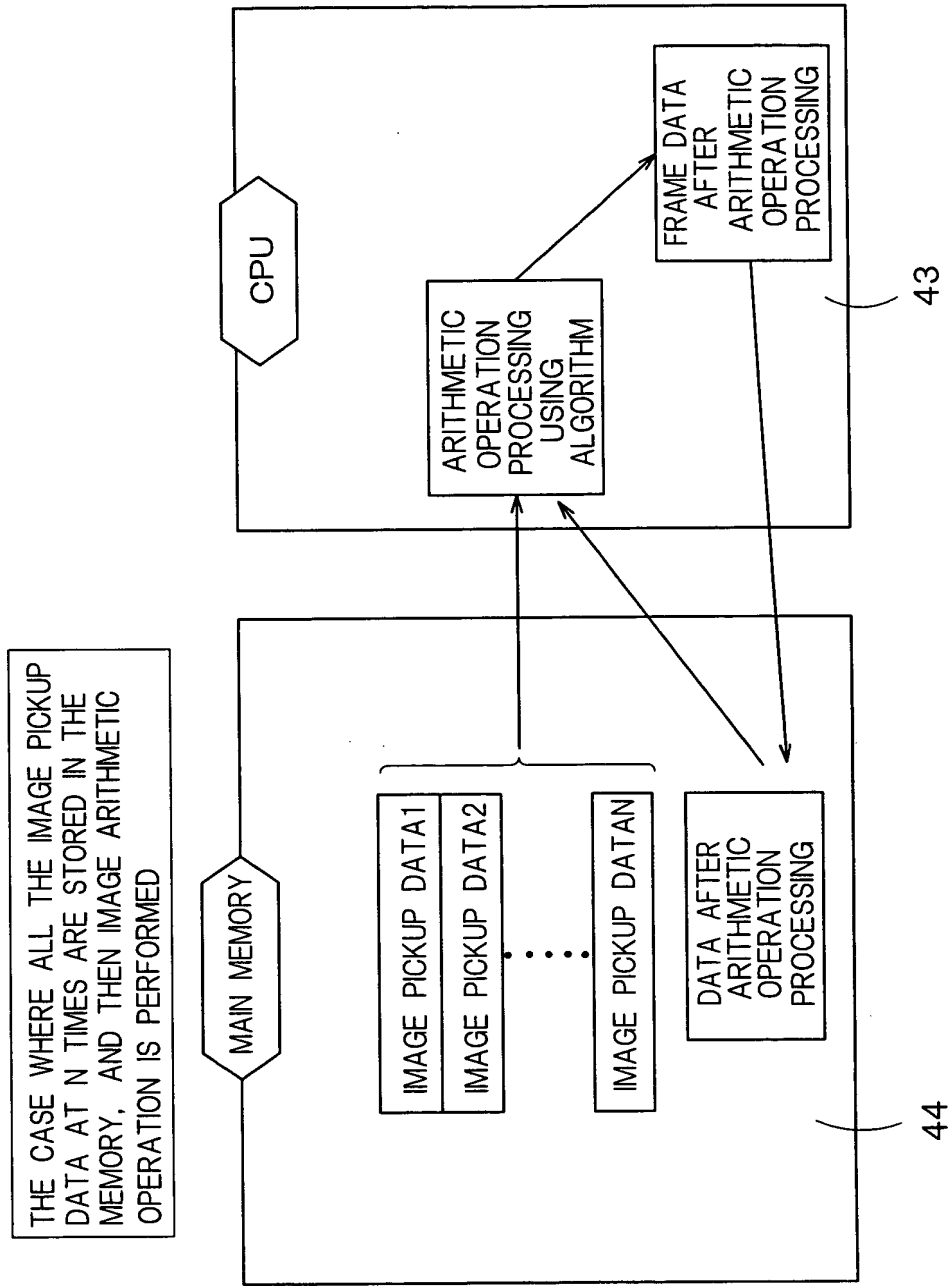


FIG. 15

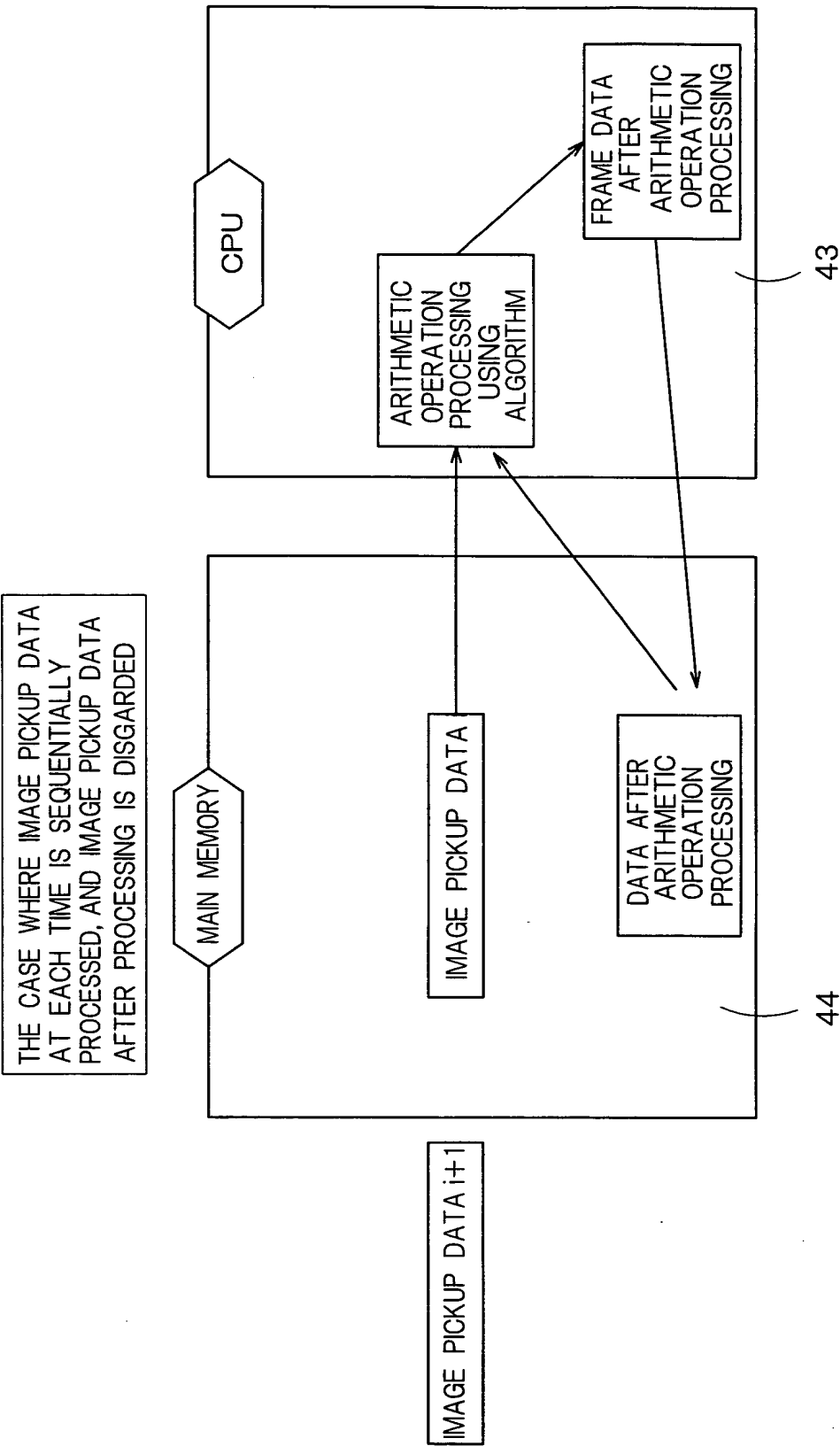


FIG. 16

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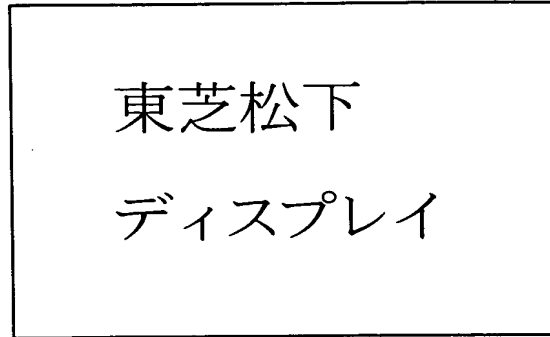


FIG. 17A

東芝松下

ディスプレイ

FIG. 17B

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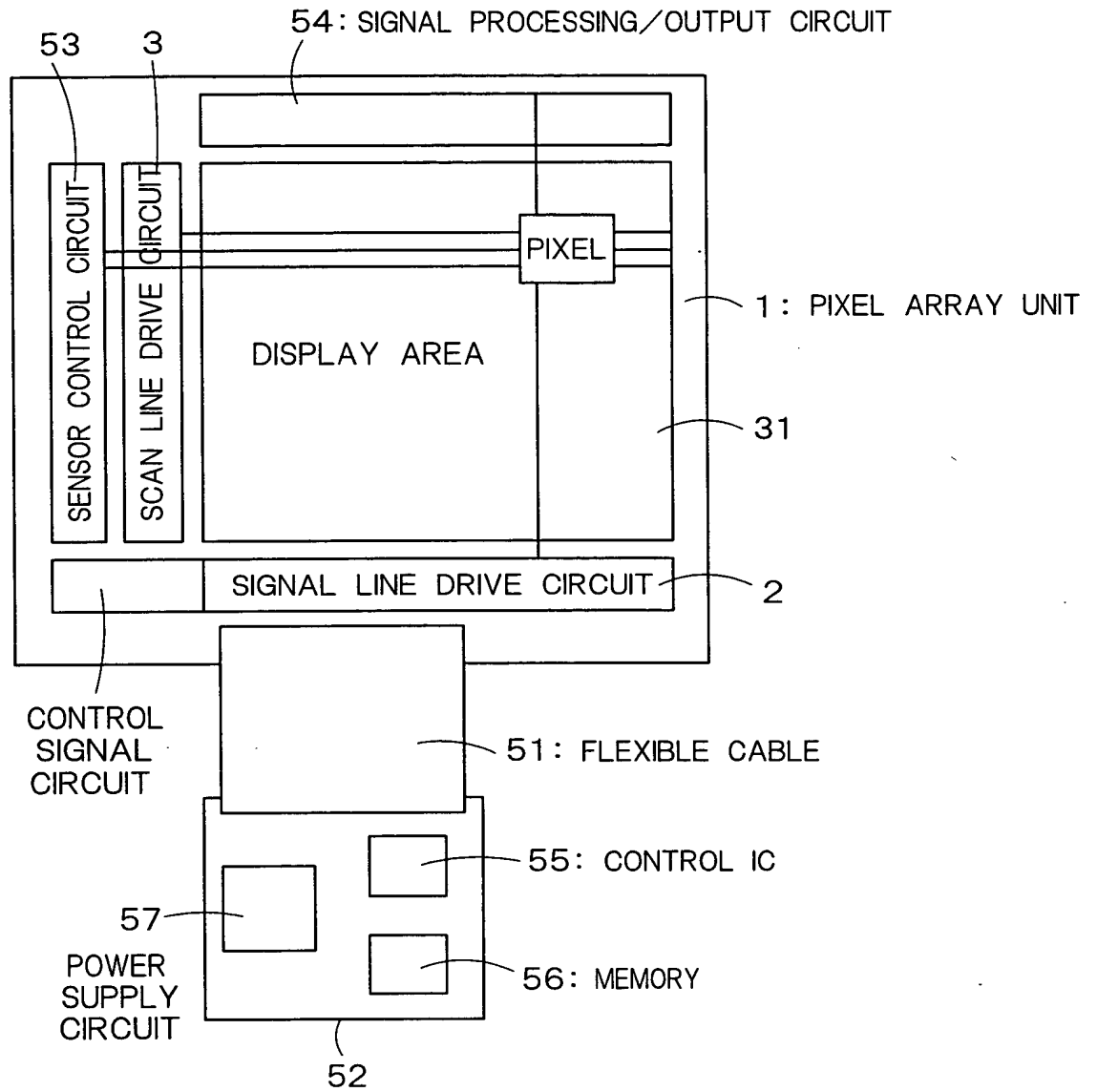


FIG. 18





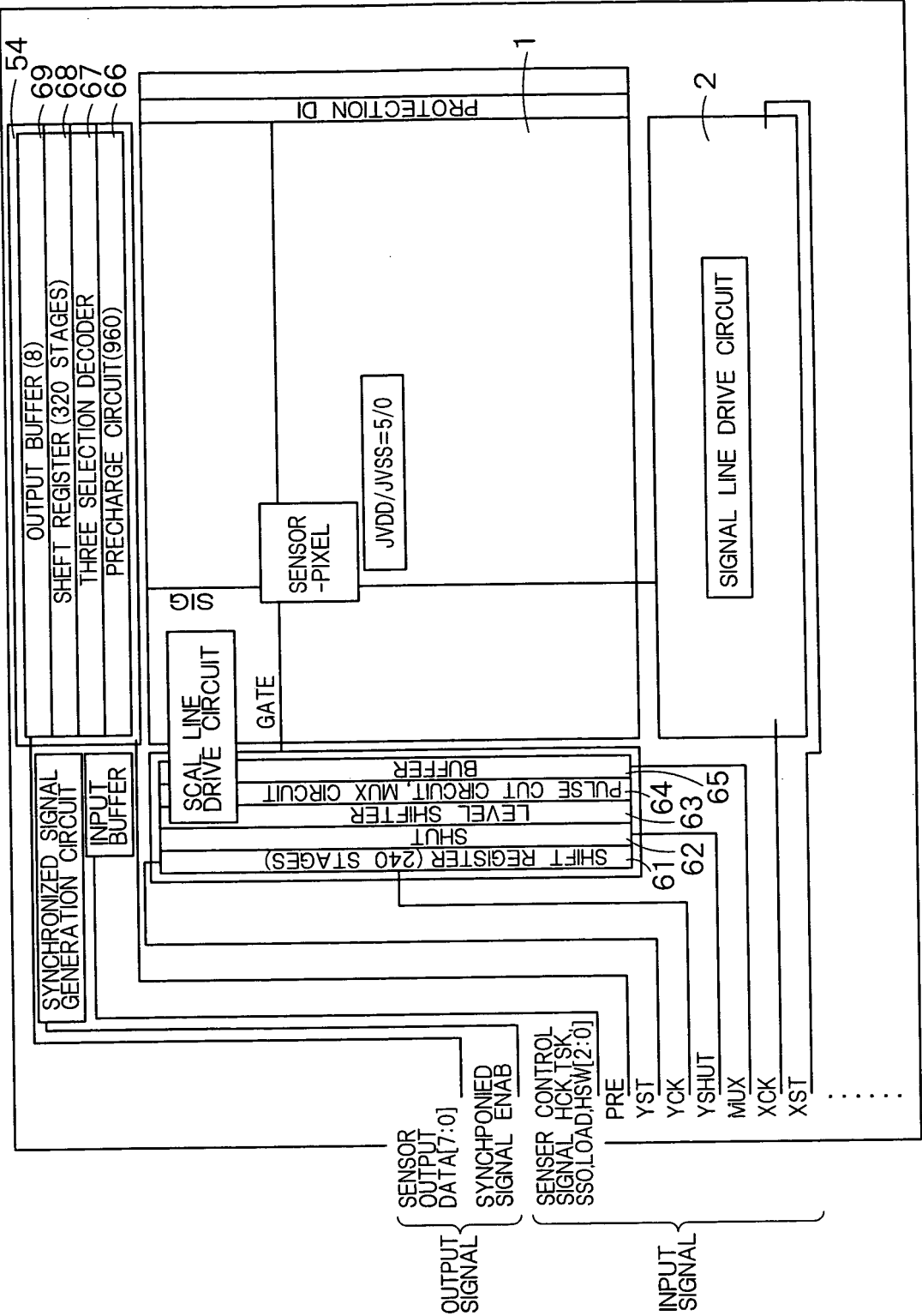


FIG. 20

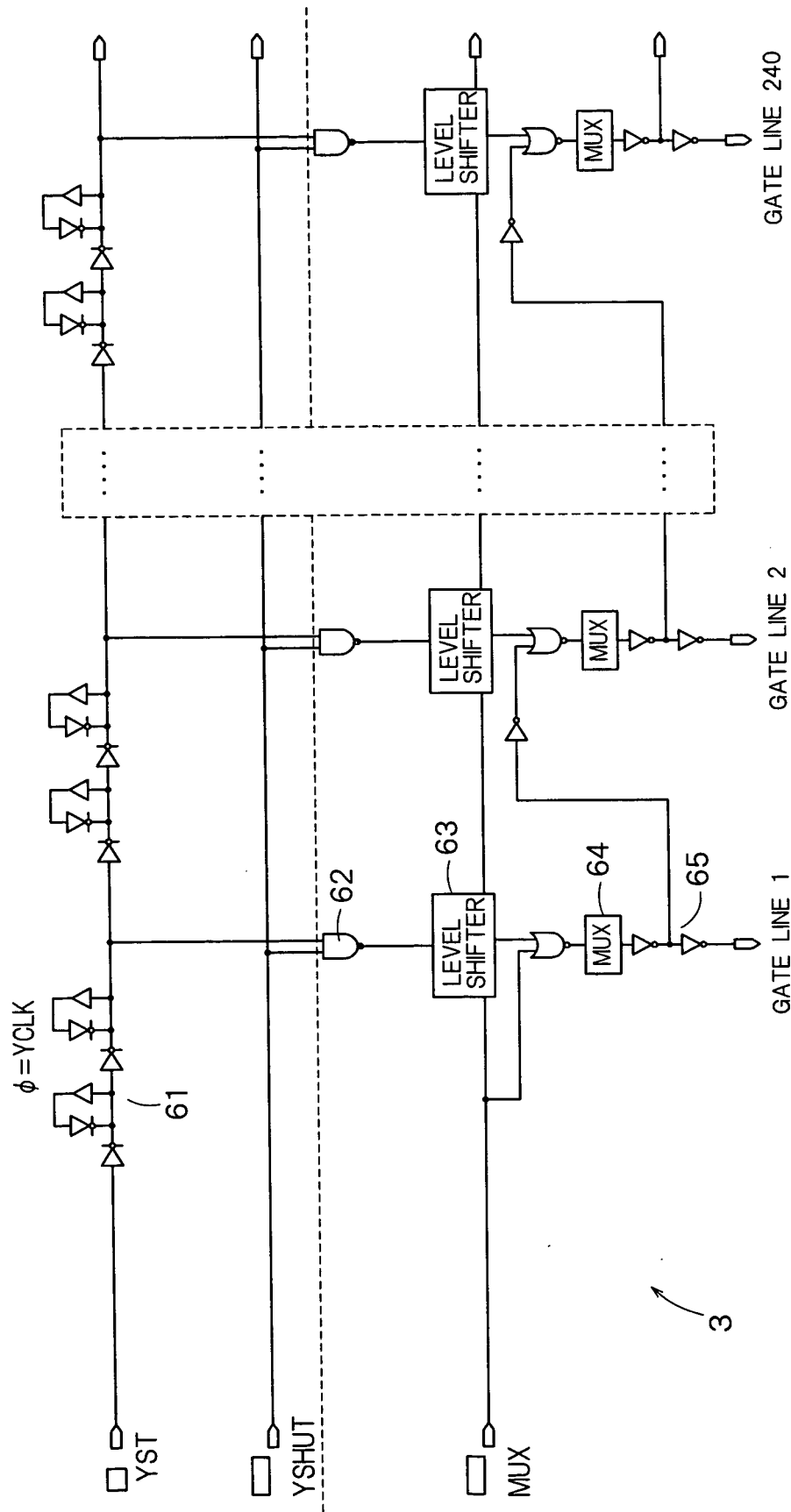


FIG. 21

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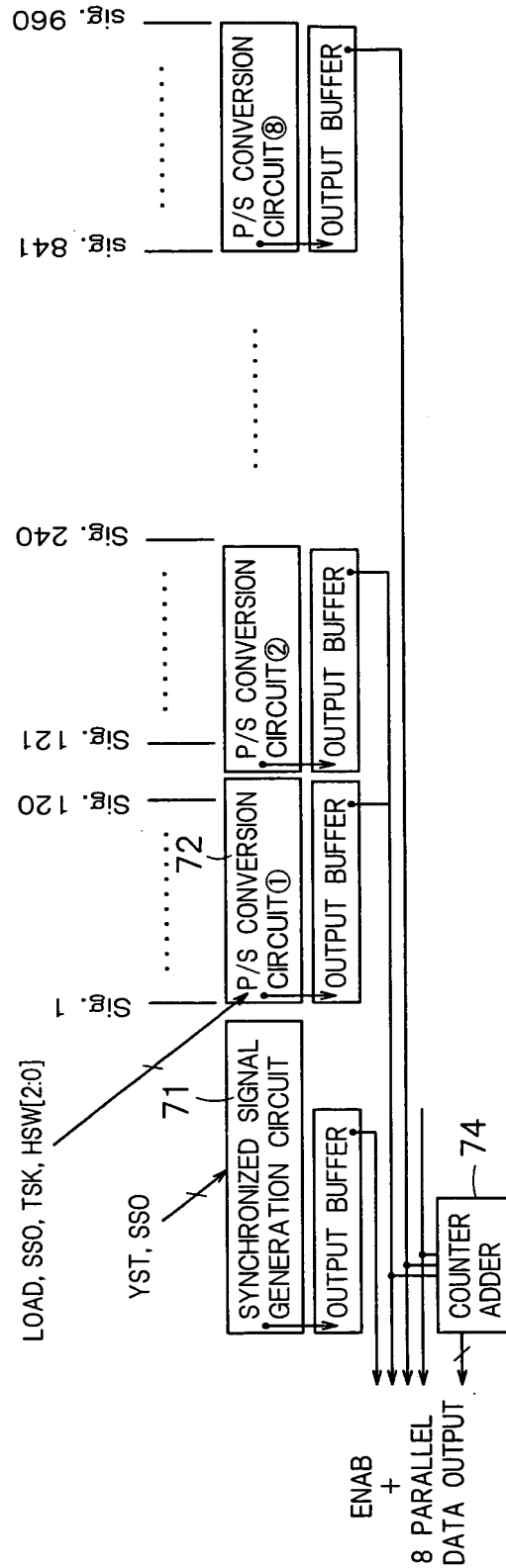


FIG. 22

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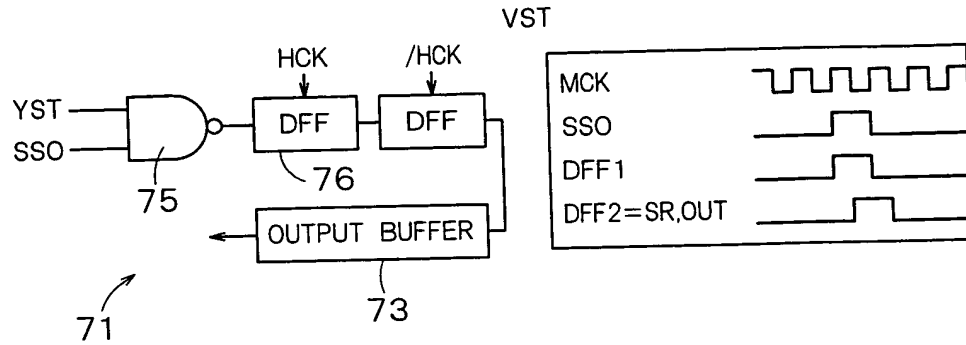


FIG. 23

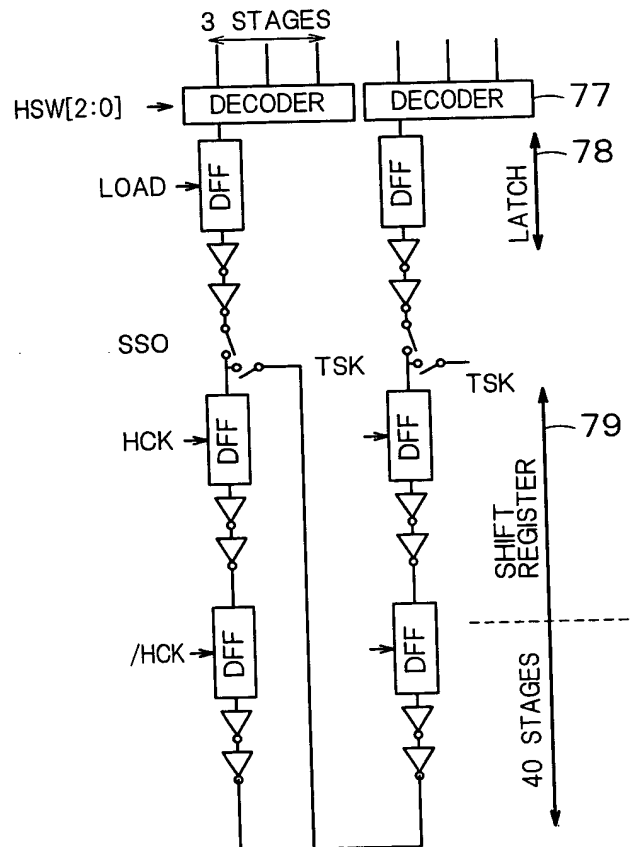


FIG. 24

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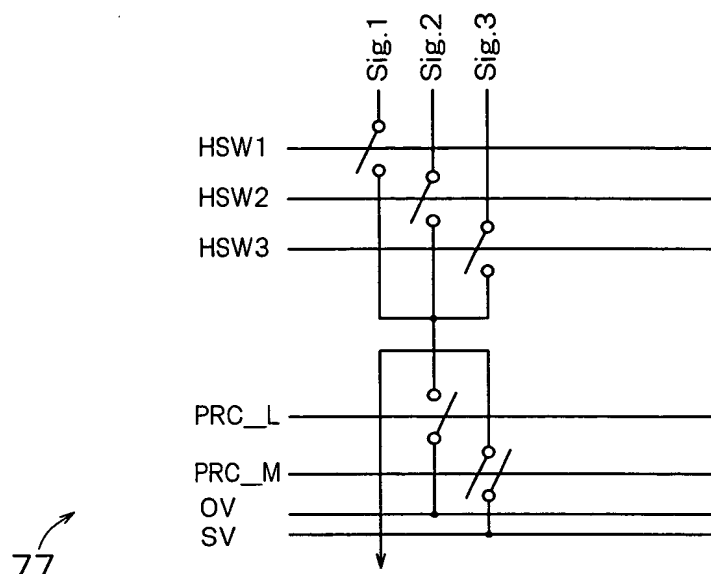
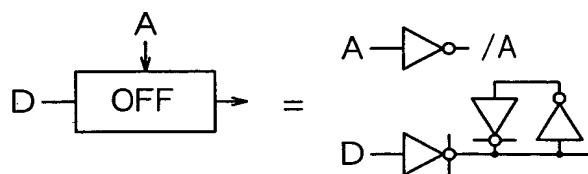
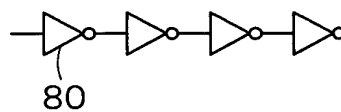


FIG. 25



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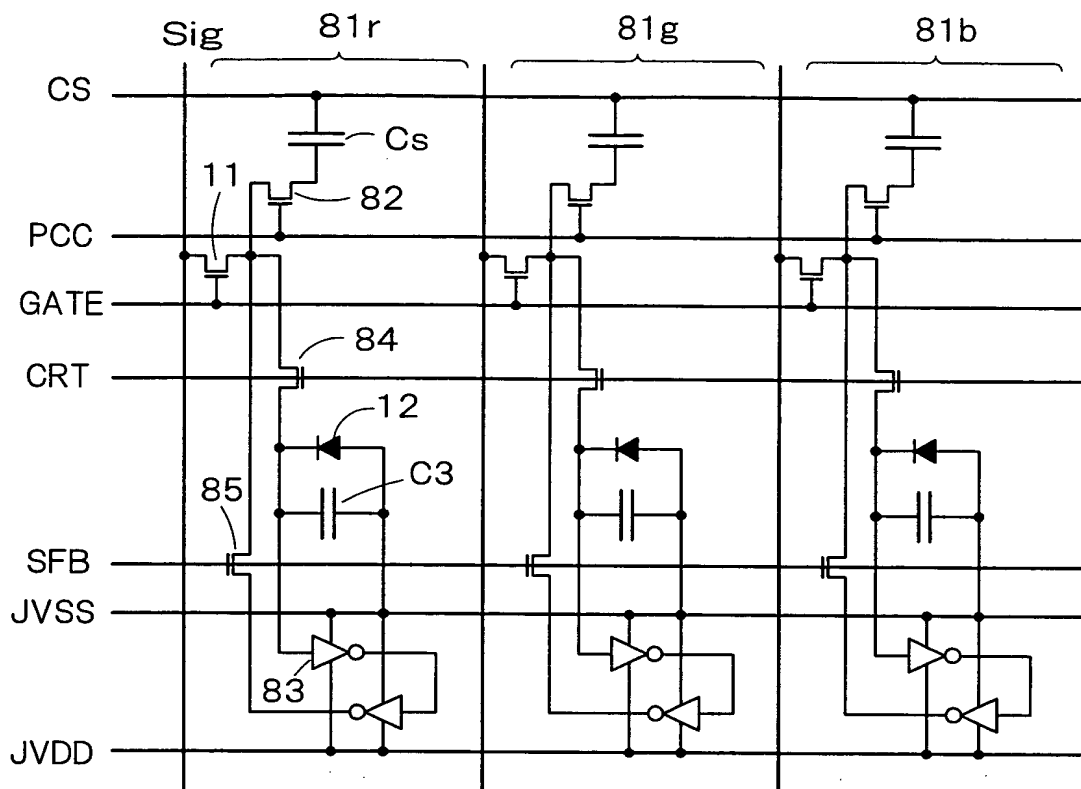
FIG. 26



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FIG. 27

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PCC...PIXEL Cs CONNECTION

SFB...SRAM FEED BACK

CRT...CAPACITOR RESET TRANSISTOR

FIG. 28

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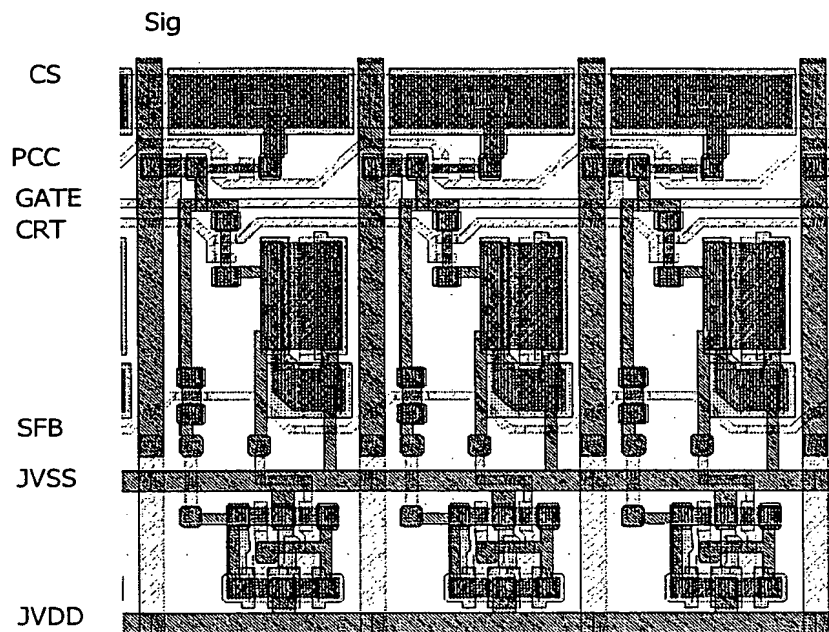


FIG. 29



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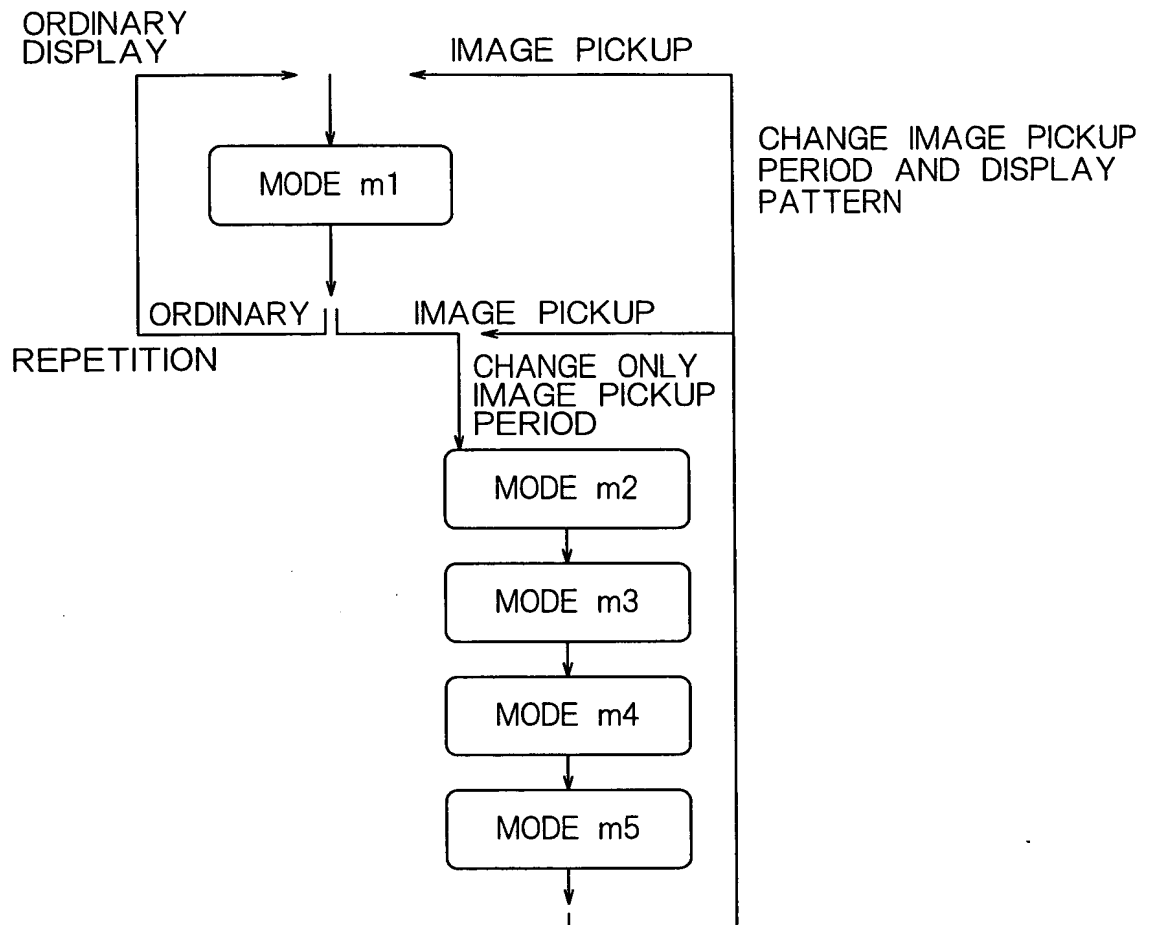


FIG. 30

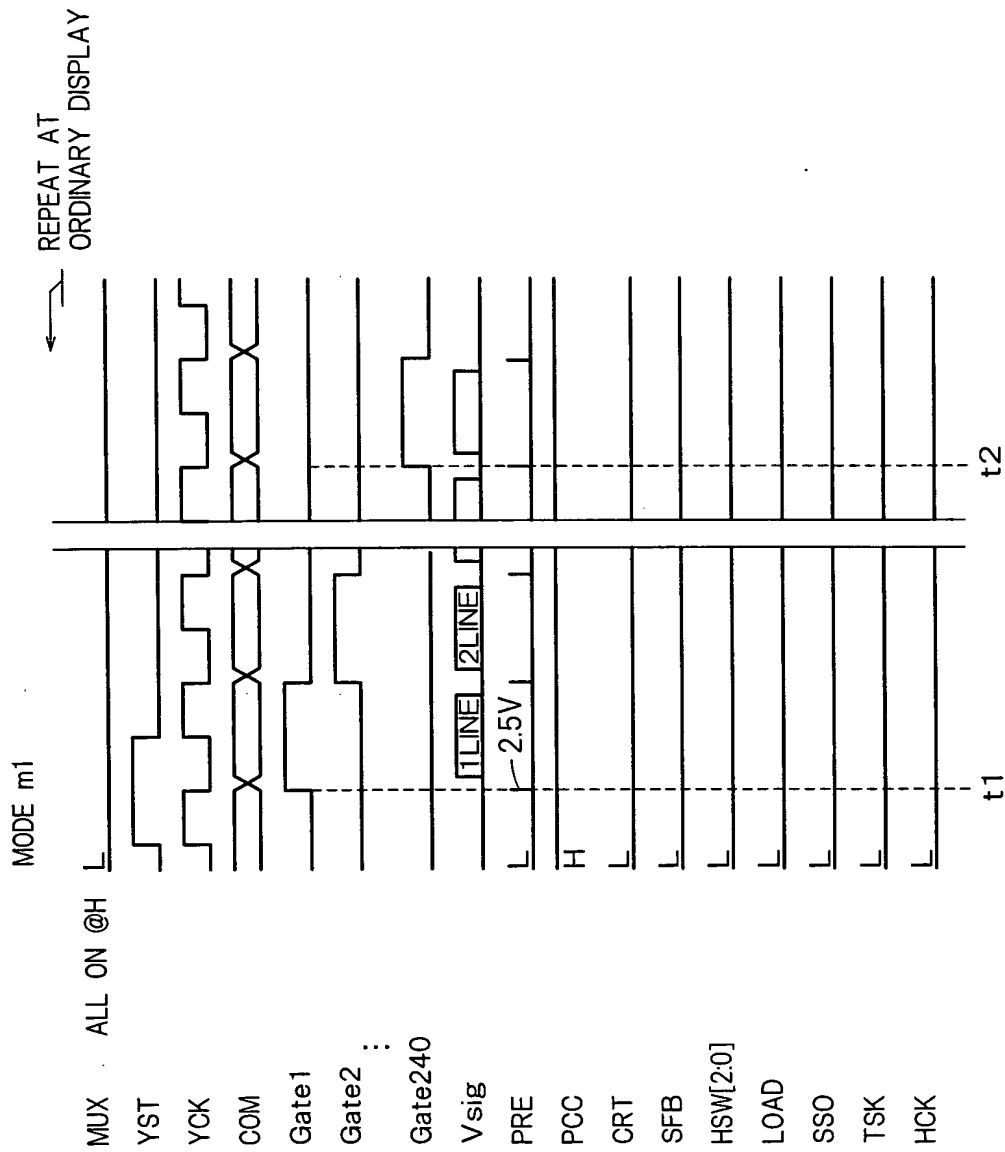


FIG. 31

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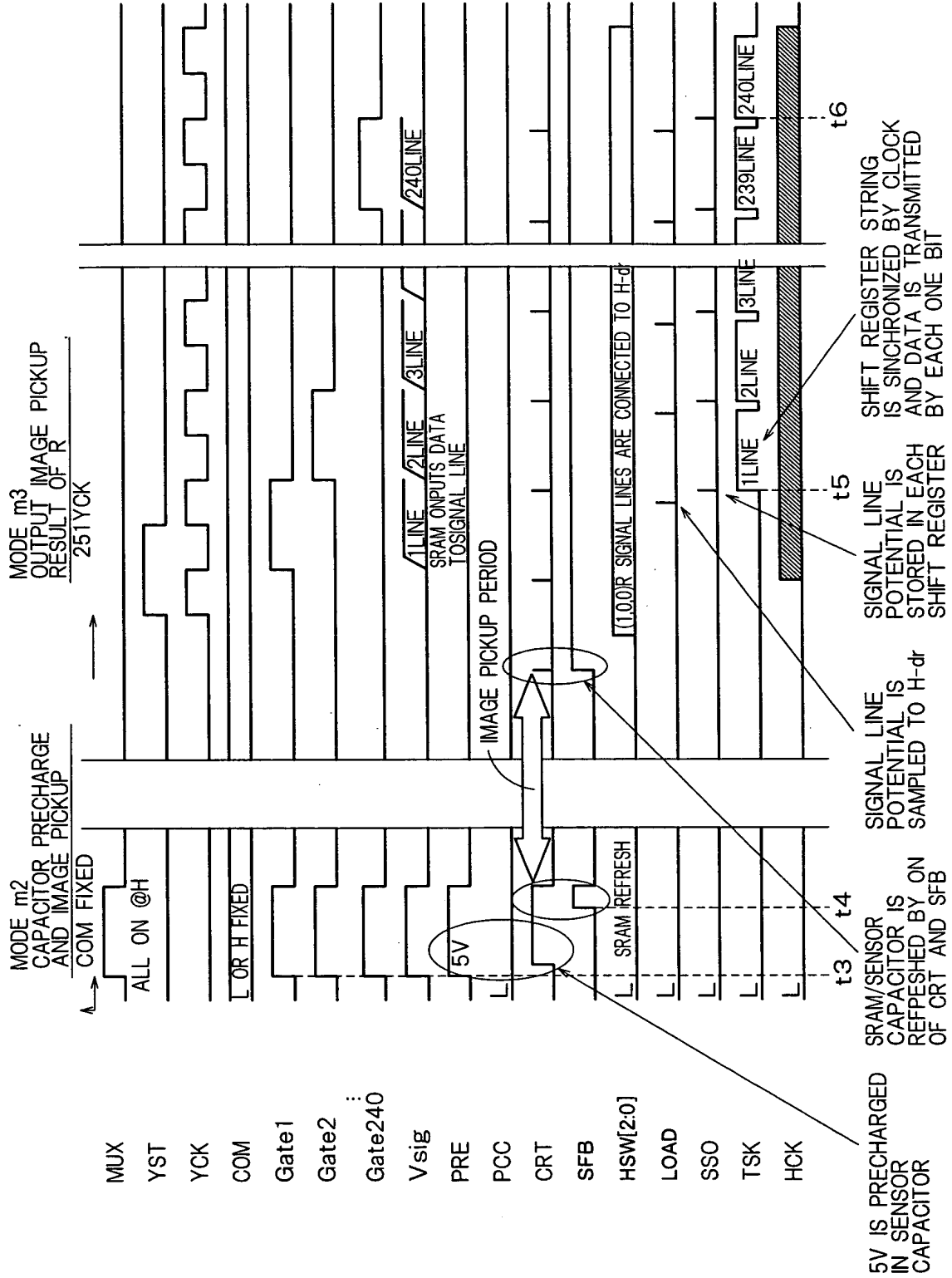


FIG. 32

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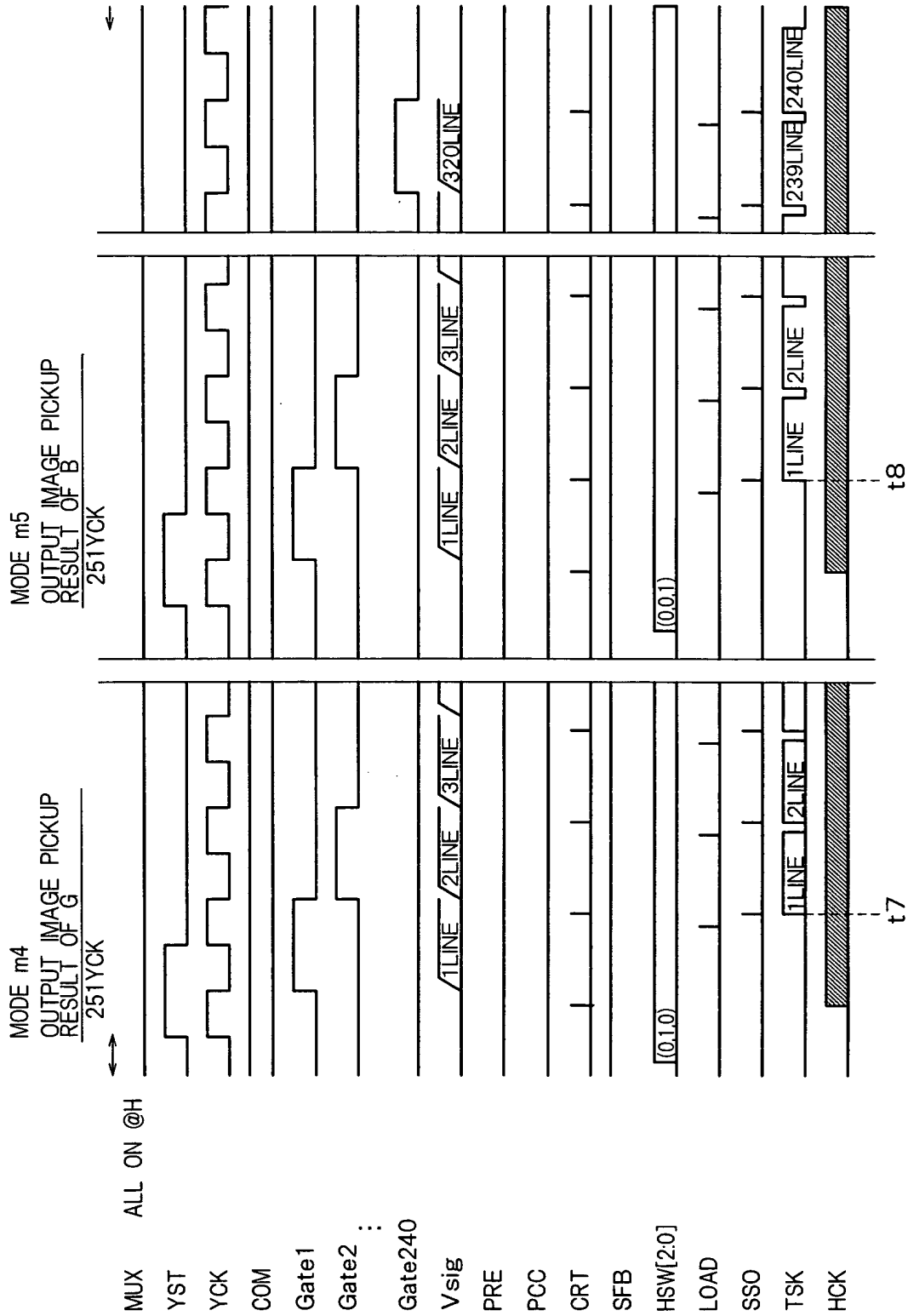


FIG. 33

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1 BLOCK = 40×30  
(HORIZONTAL 8, VERTICAL 8)

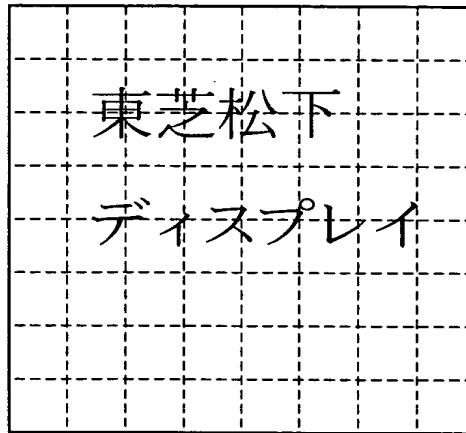


FIG. 34

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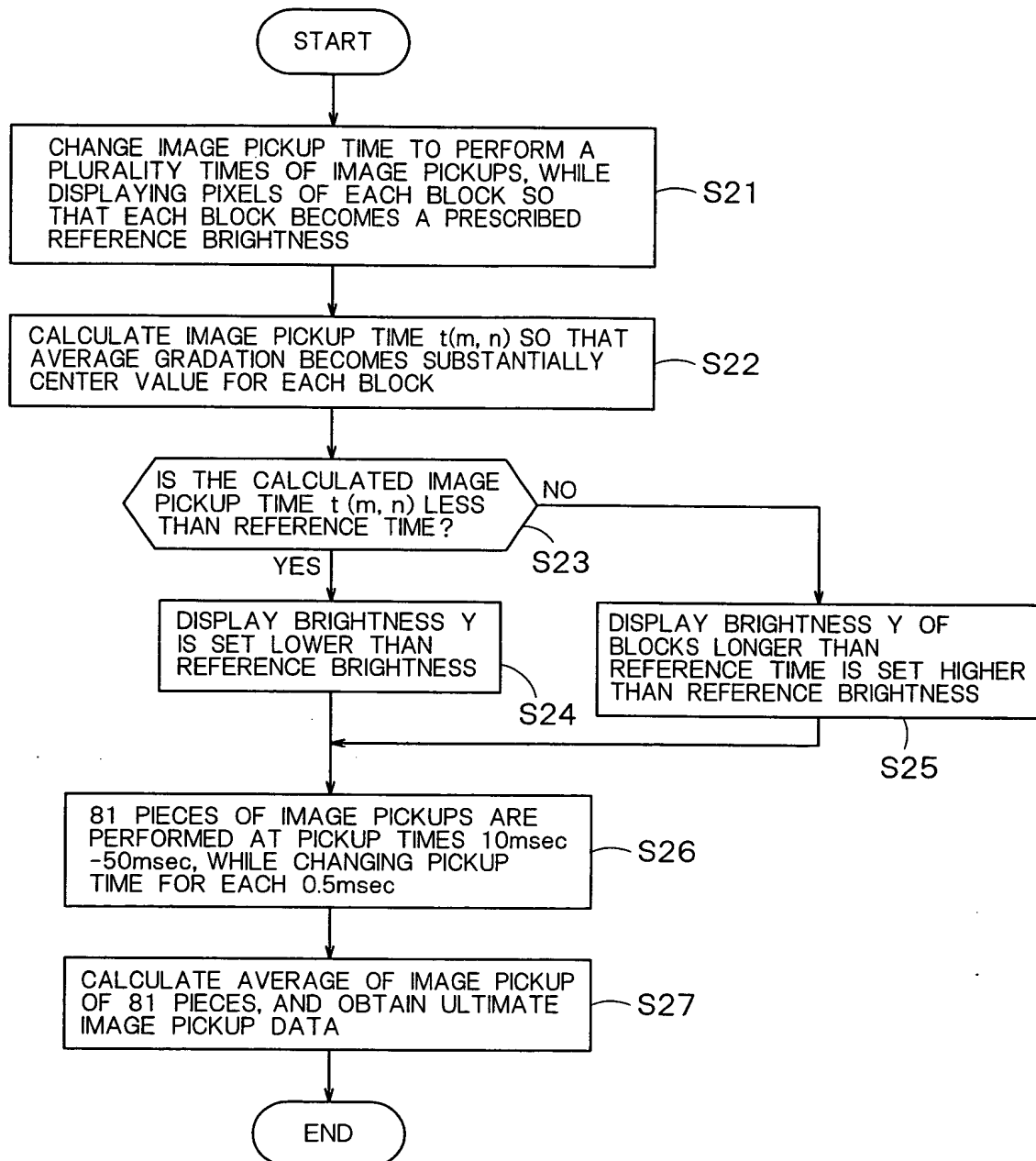


FIG. 35

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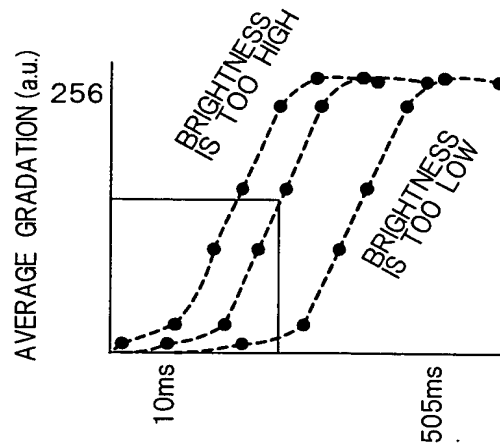


FIG. 36

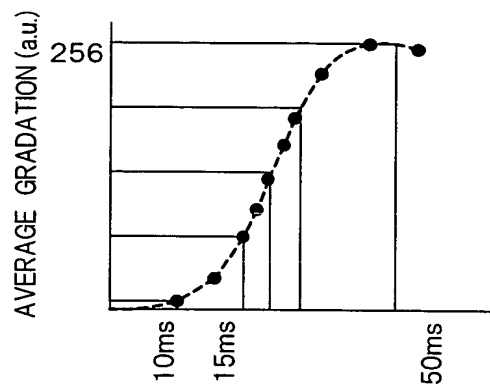


FIG. 37

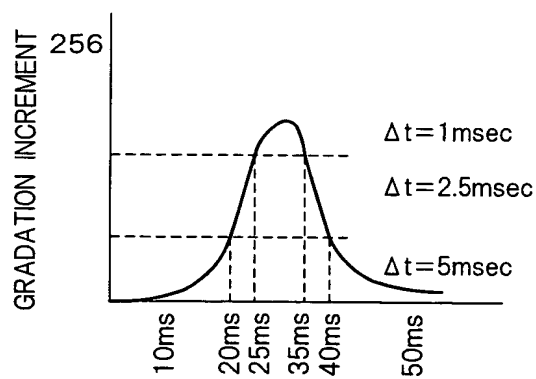


FIG. 38

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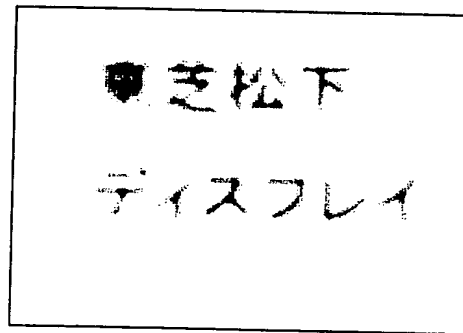


FIG. 39



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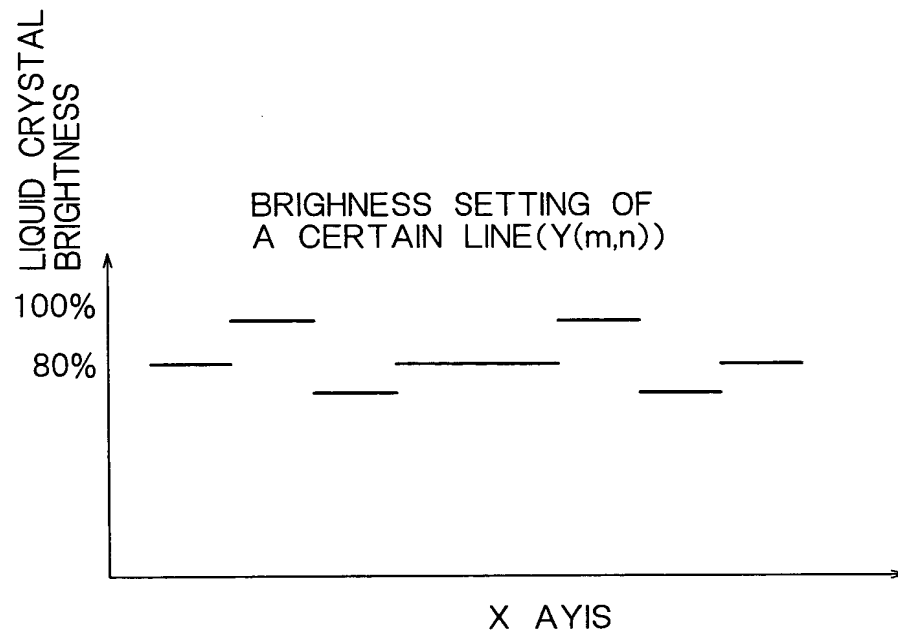


FIG. 40



FIG. 41

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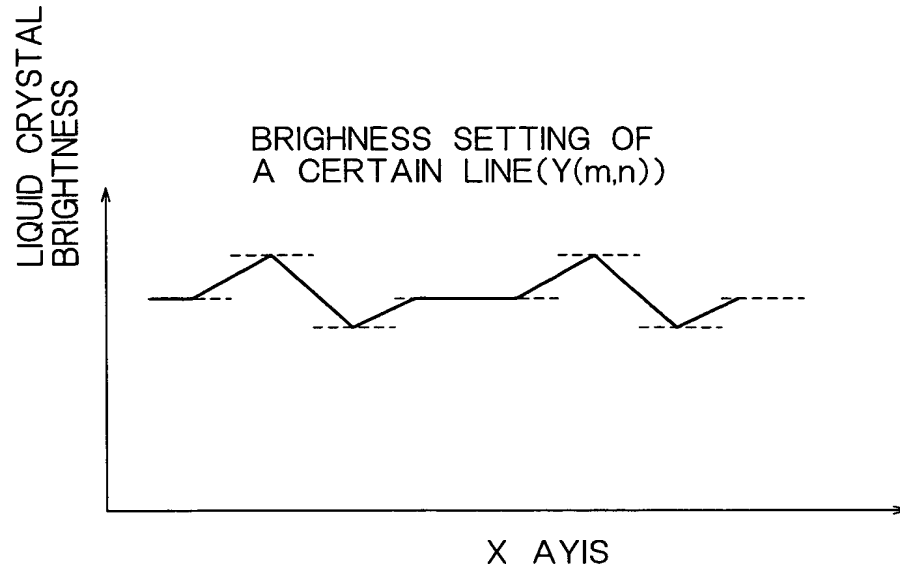


FIG. 42



FIG. 43

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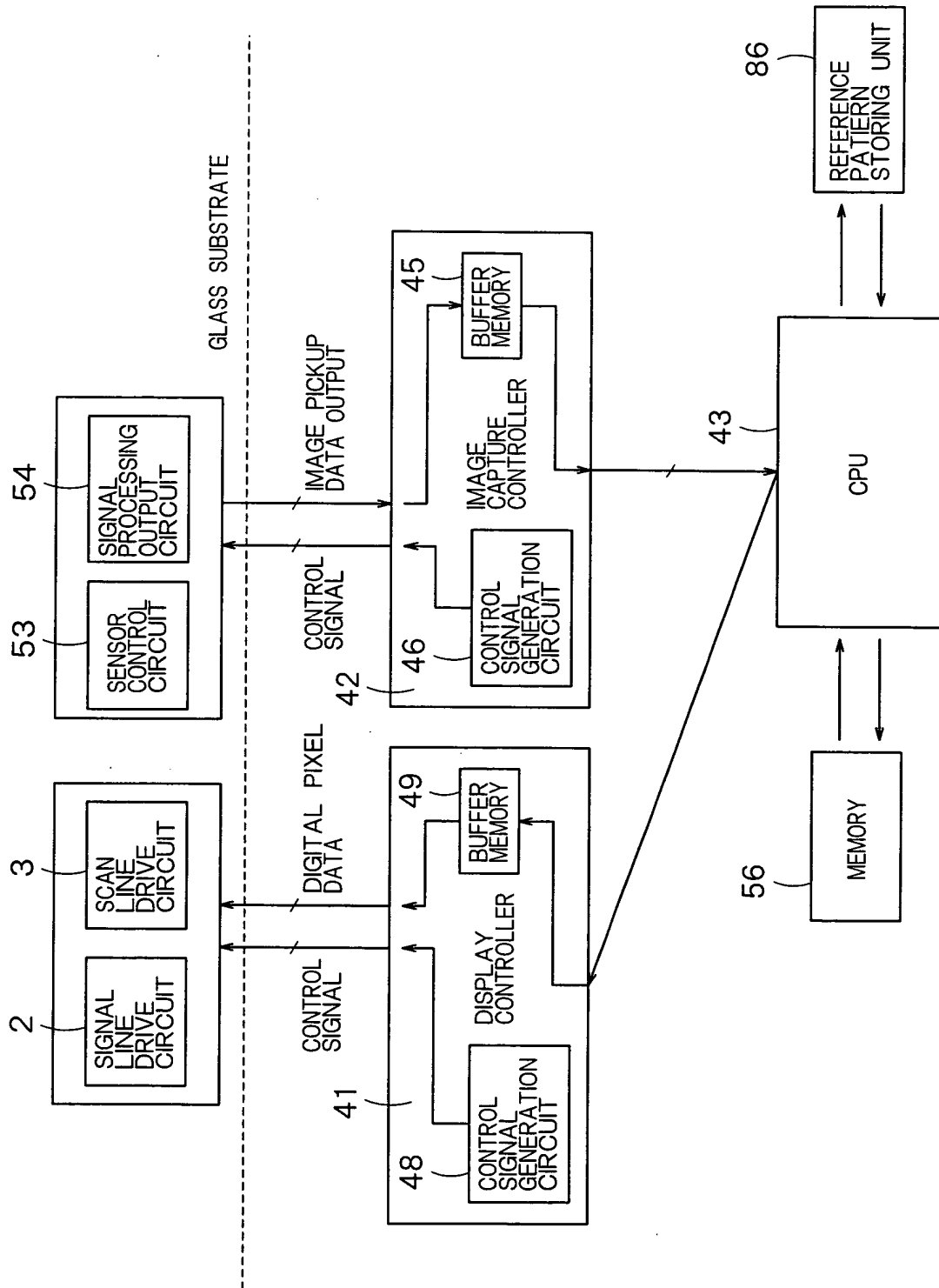


FIG. 44

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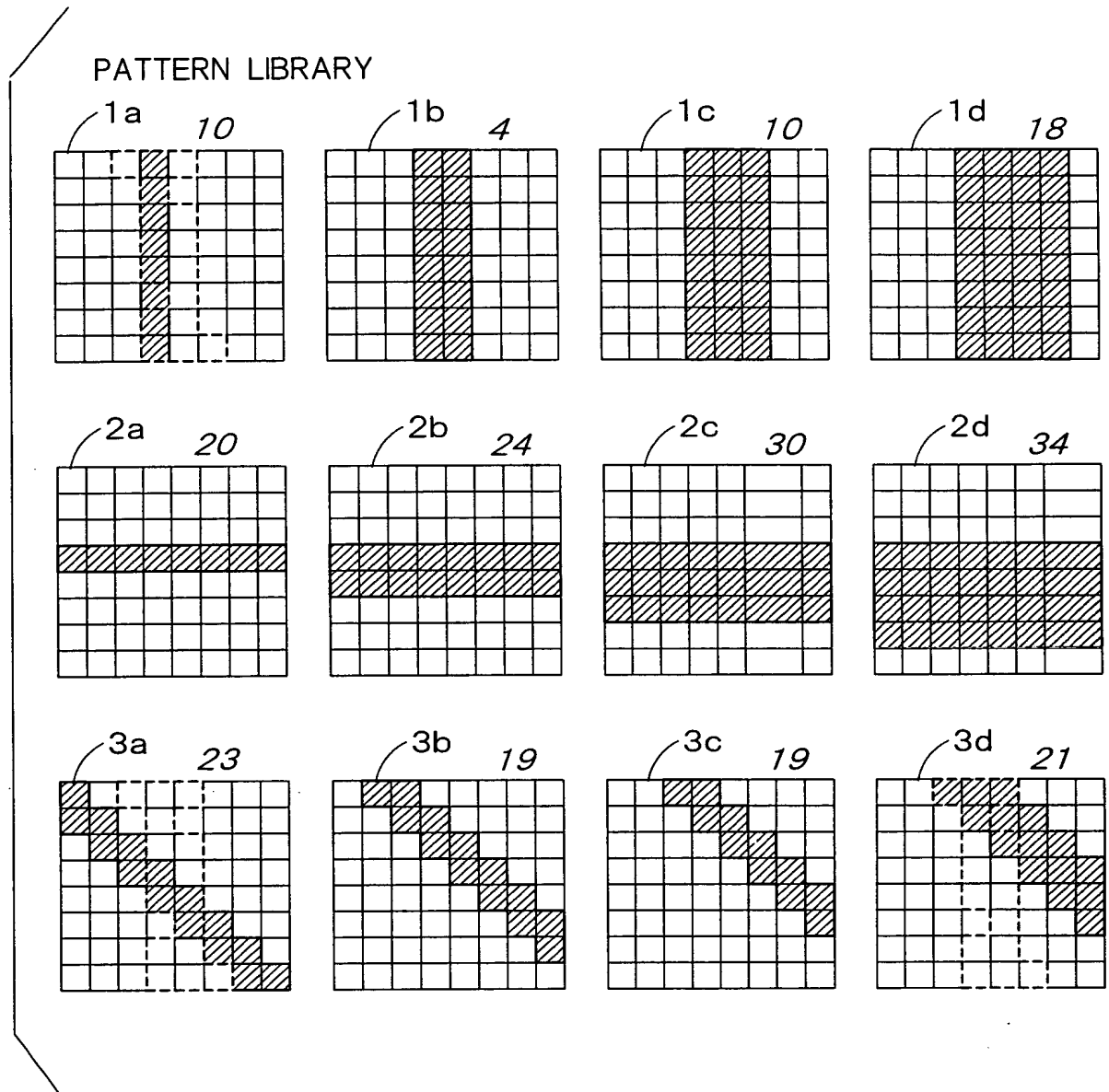


FIG. 45

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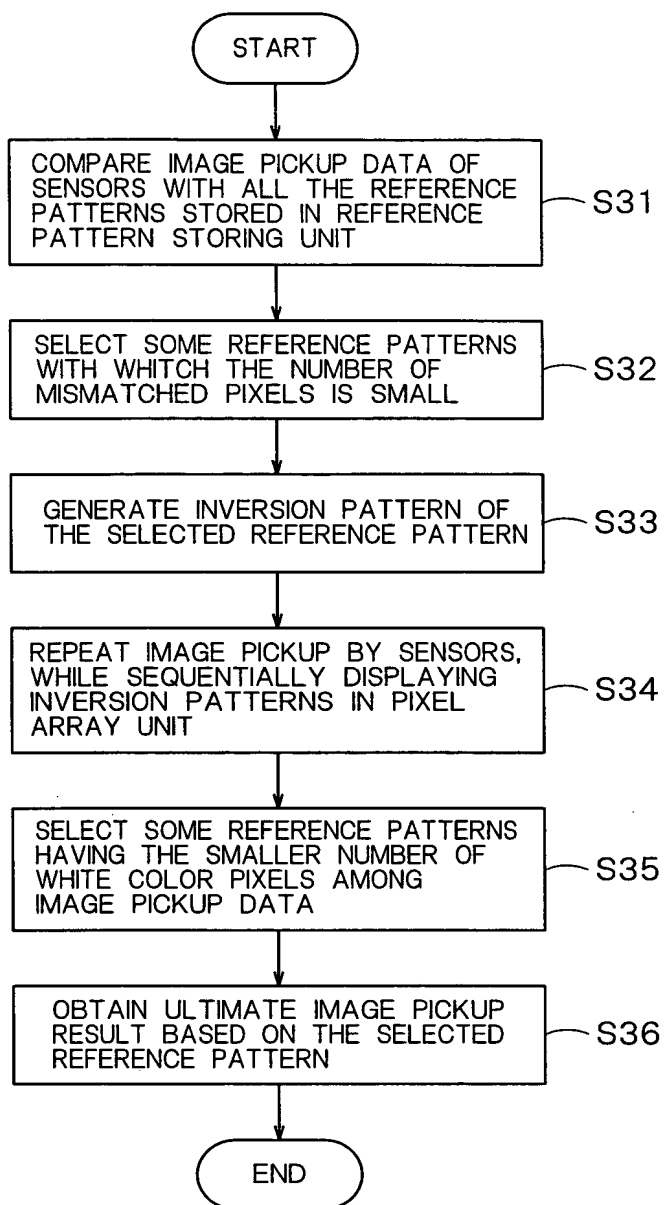


FIG. 46

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IMAGE PICKUP OBJECT

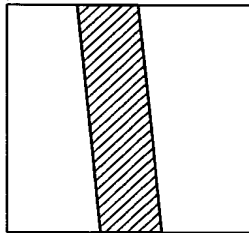


FIG. 47

IMAGE PICKUP RESULT

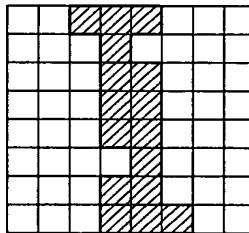


FIG. 48

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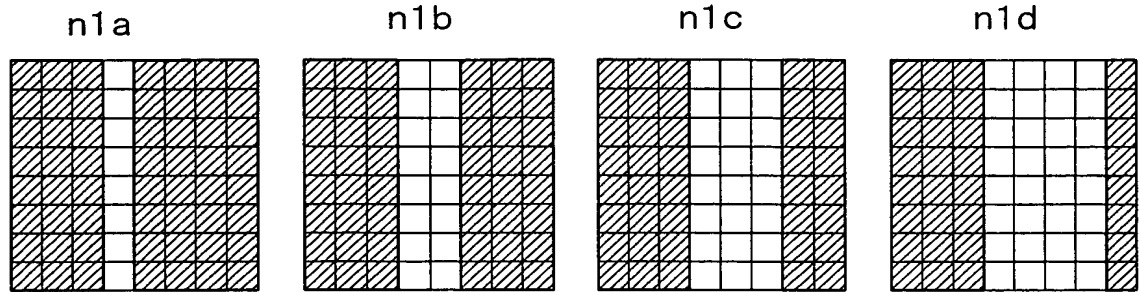


FIG. 49

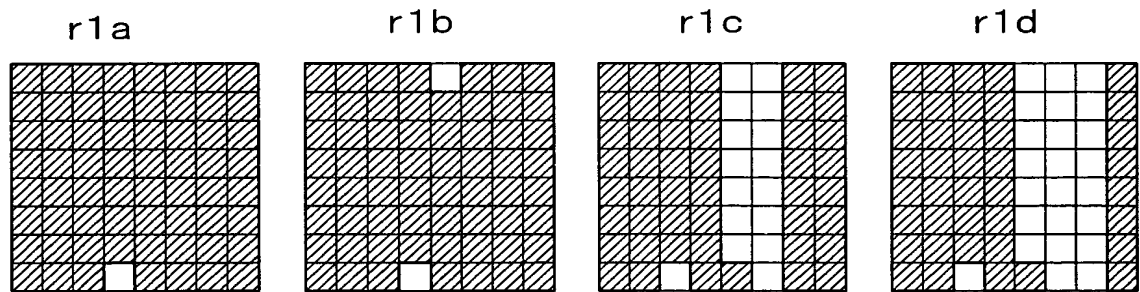


FIG. 50

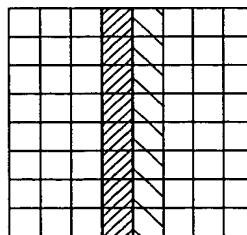


FIG. 51

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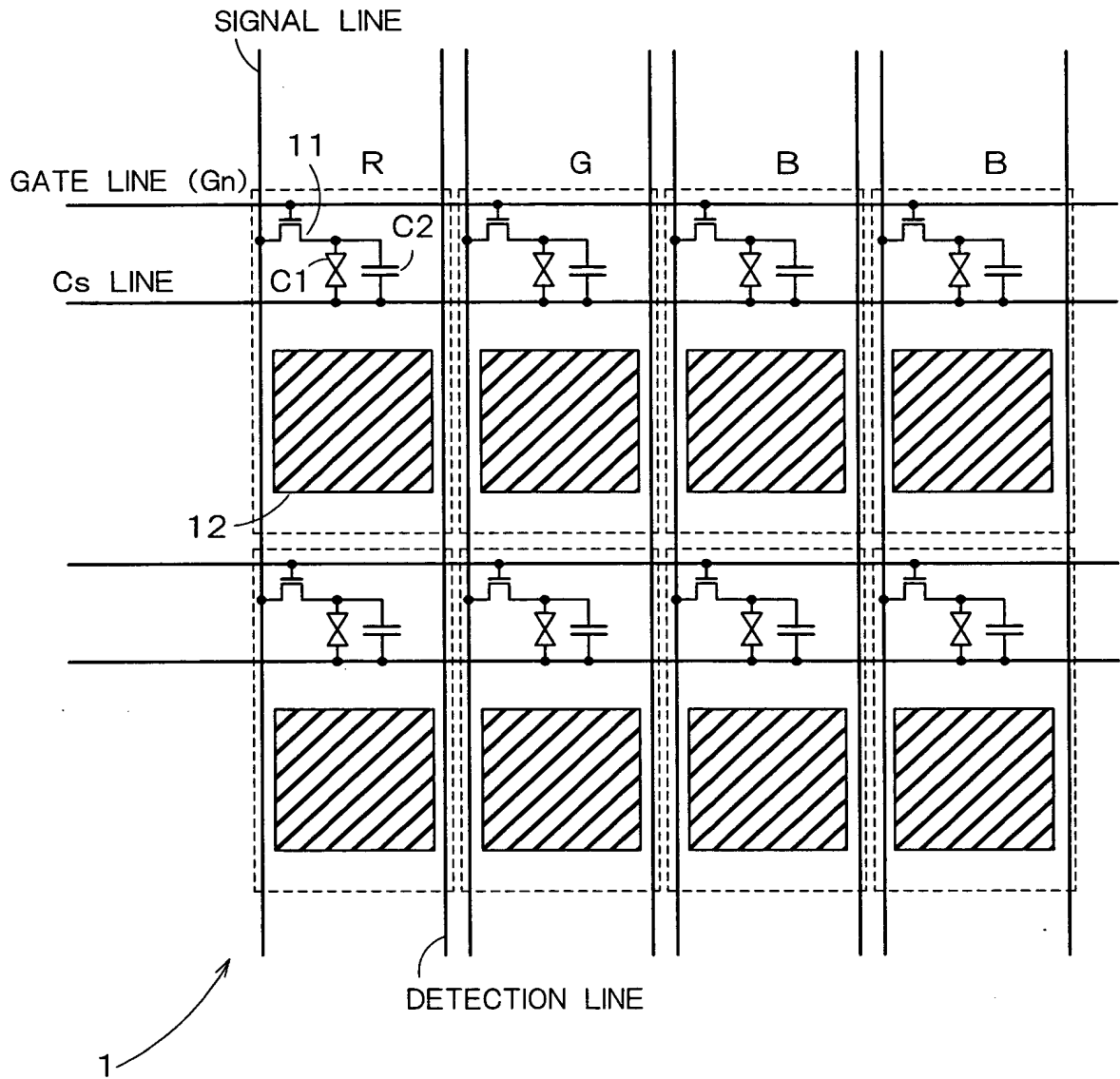


FIG. 52



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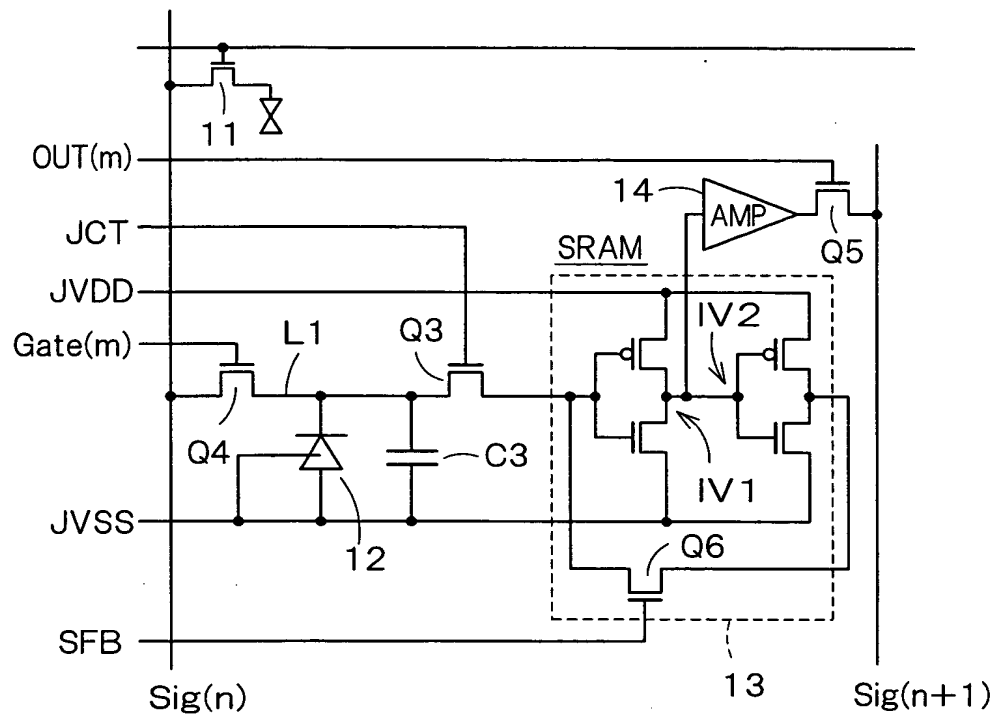


FIG. 53

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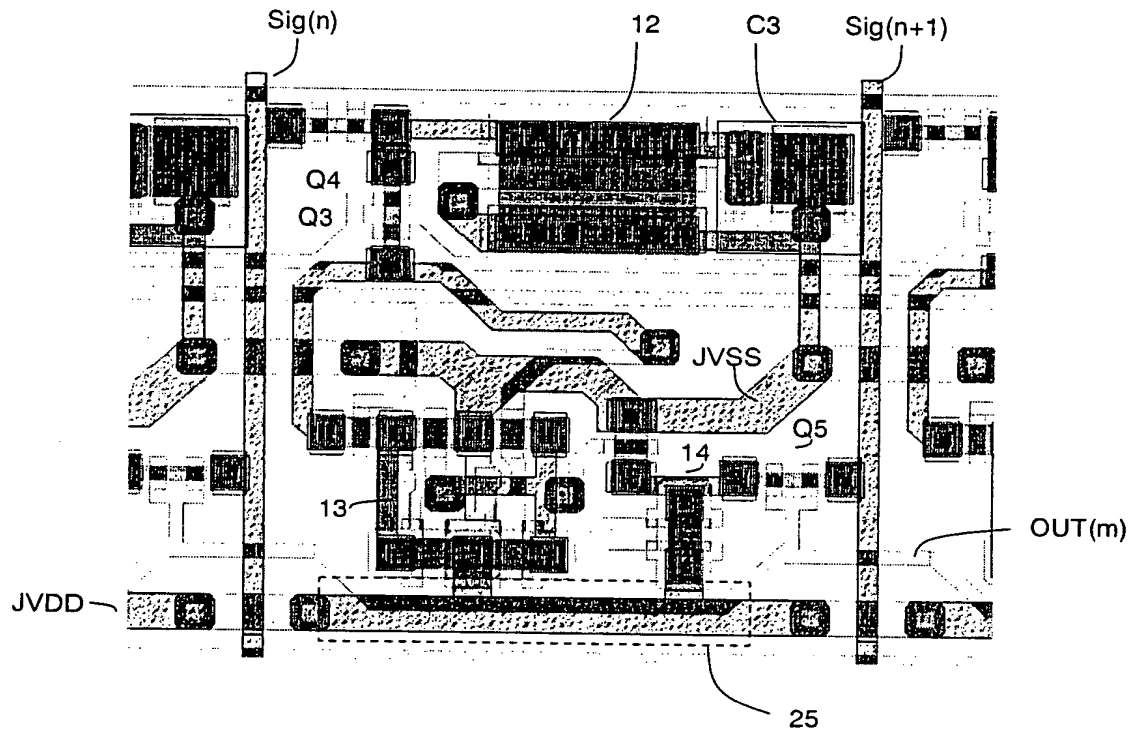
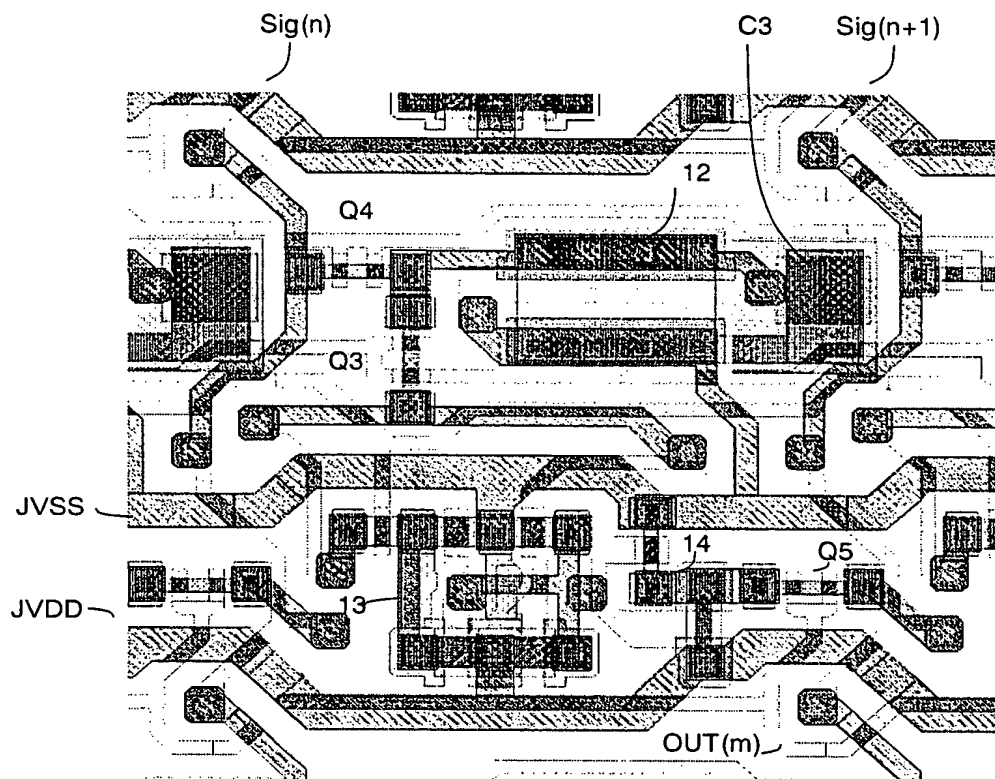


FIG. 54

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JVDD, JVSS...PATTERNED BY ONLY FIRST METAL

Sig(n)...PATTERNED BY CONNECTING FIRST AND  
SECOND METALS TO EACH OTHER

FIG. 55

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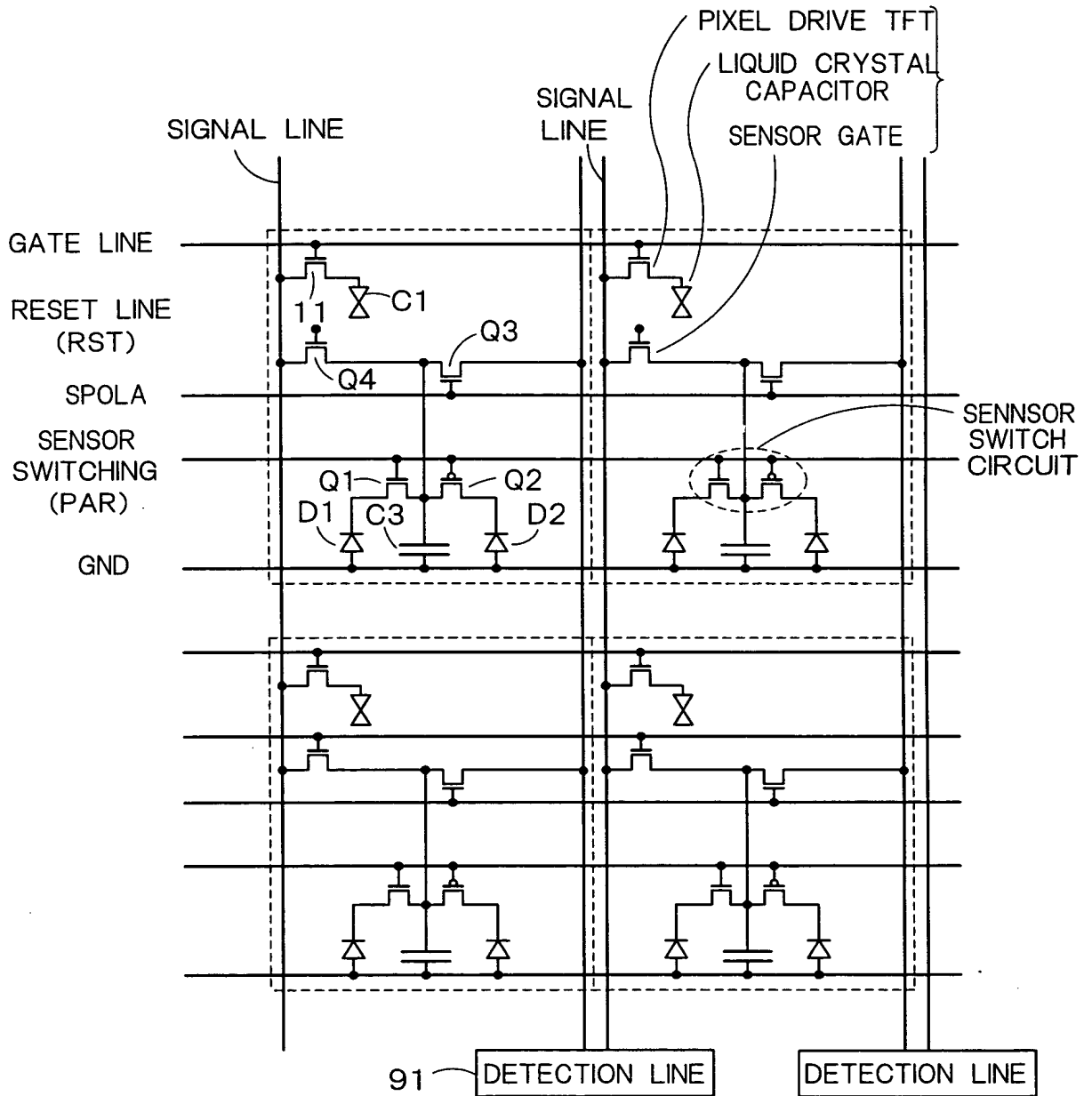


FIG. 56

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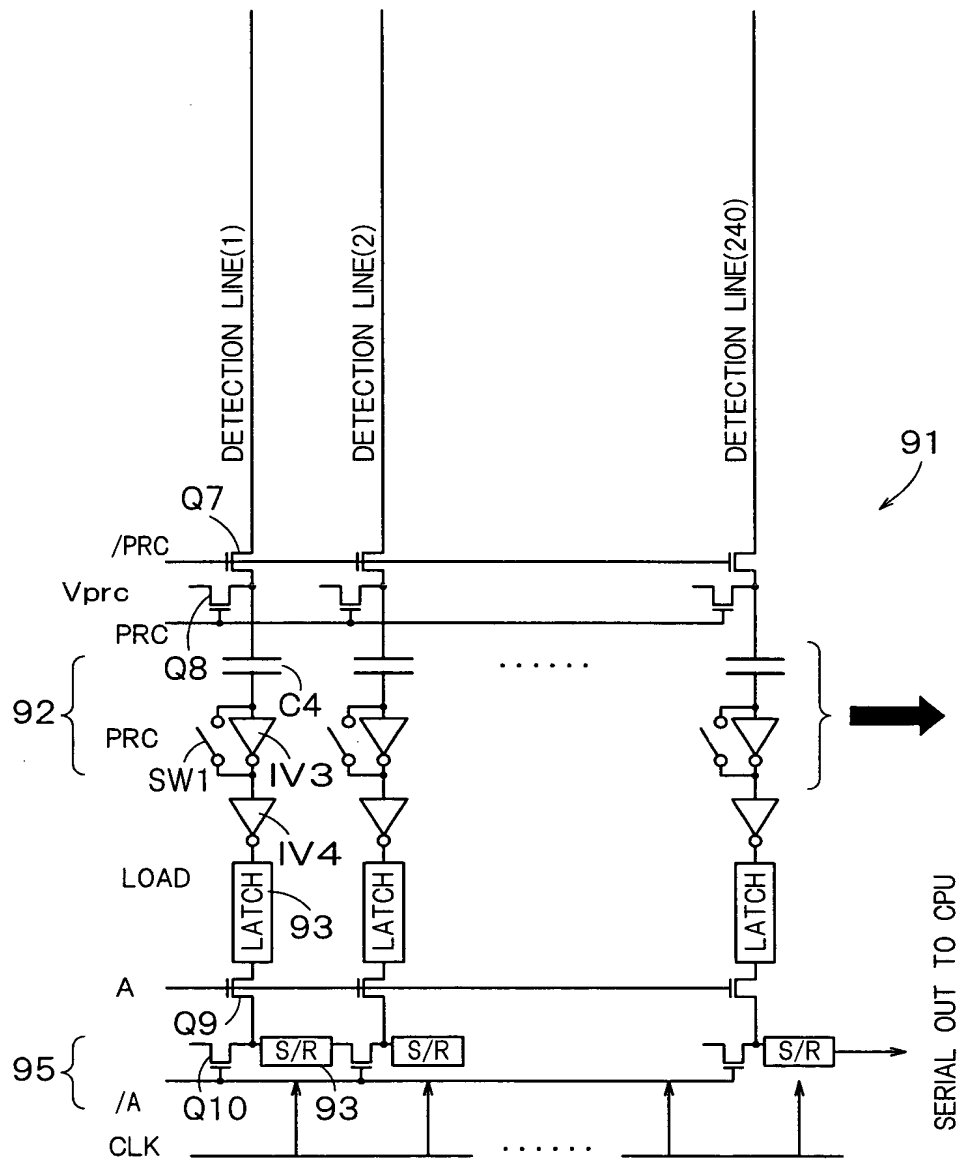


FIG. 57

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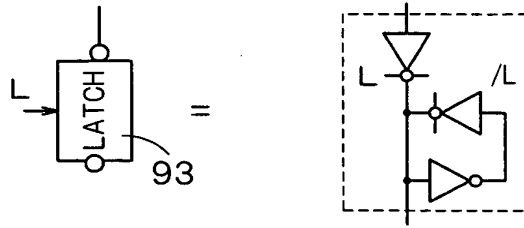


FIG. 58A

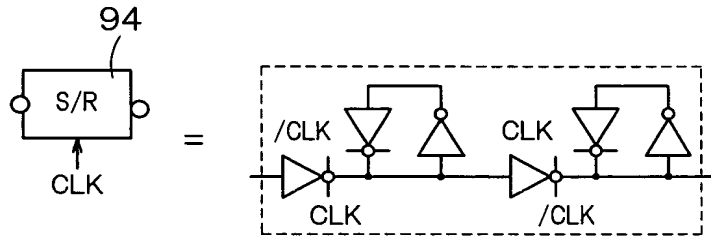


FIG. 58B

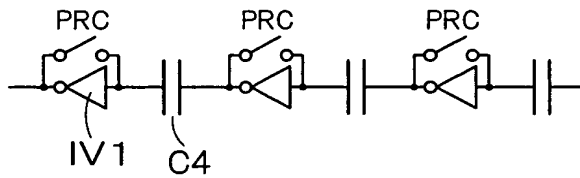


FIG. 59

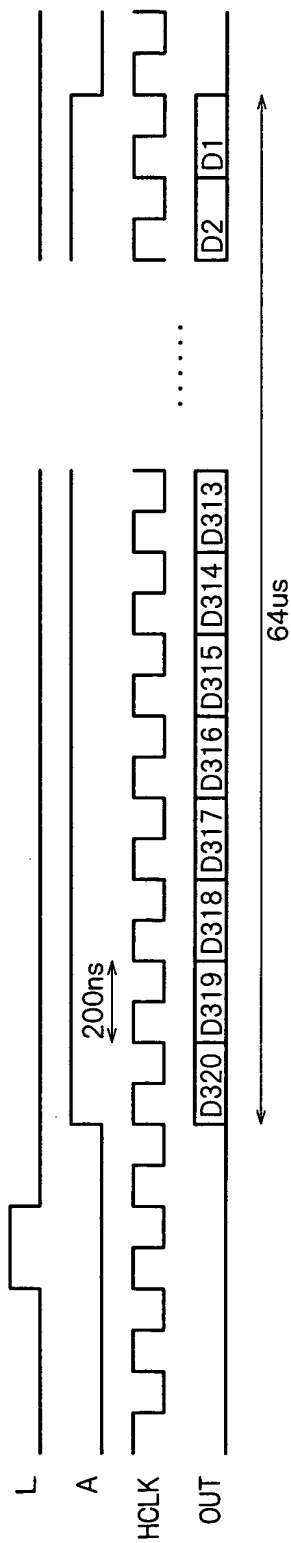


FIG. 60

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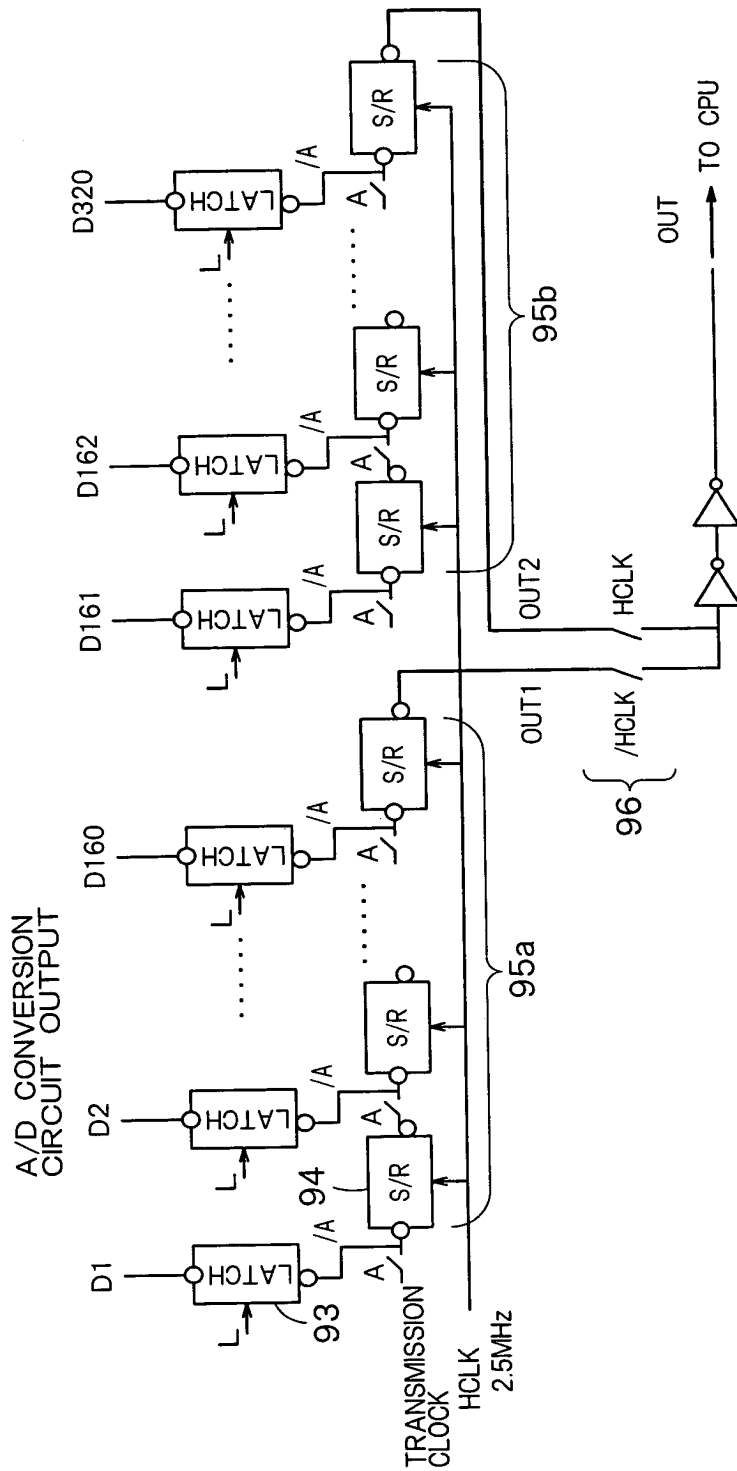


FIG. 61



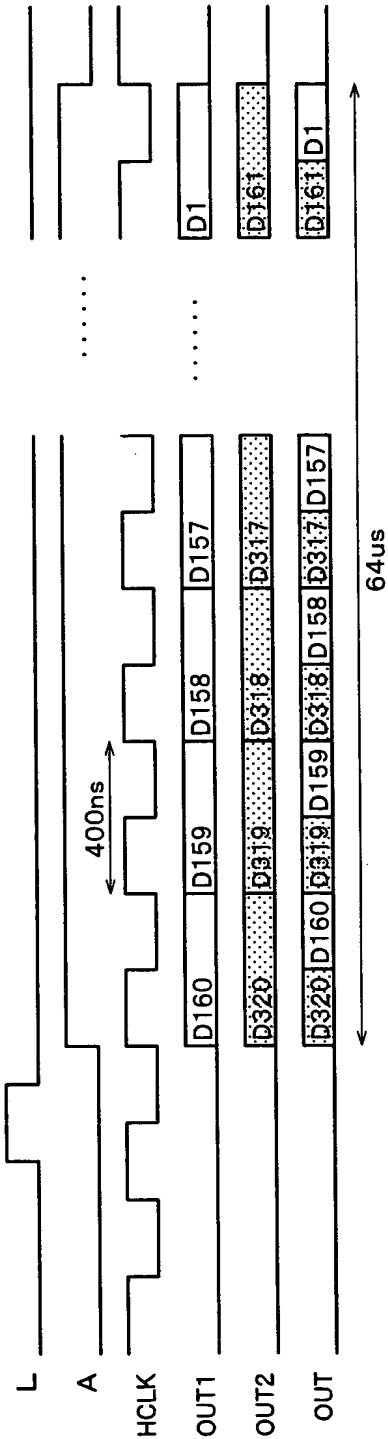
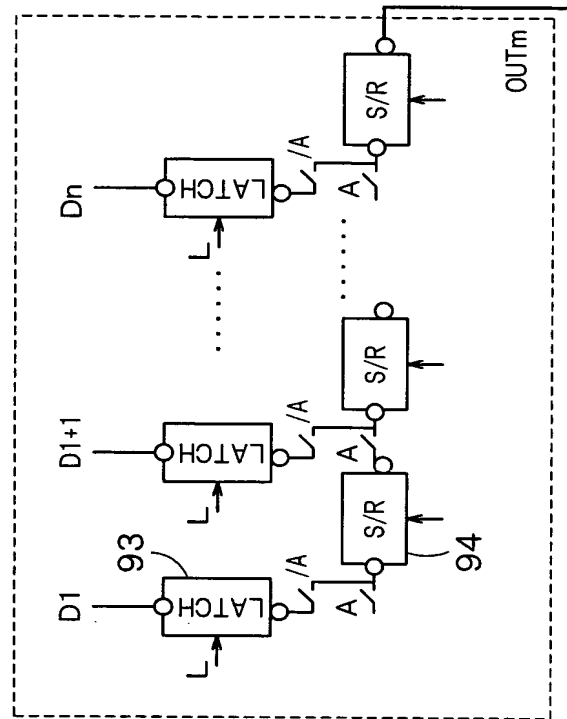


FIG. 62



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93,94

LATCH AND SHIFT  
REGISTER STRING m

FIG. 64

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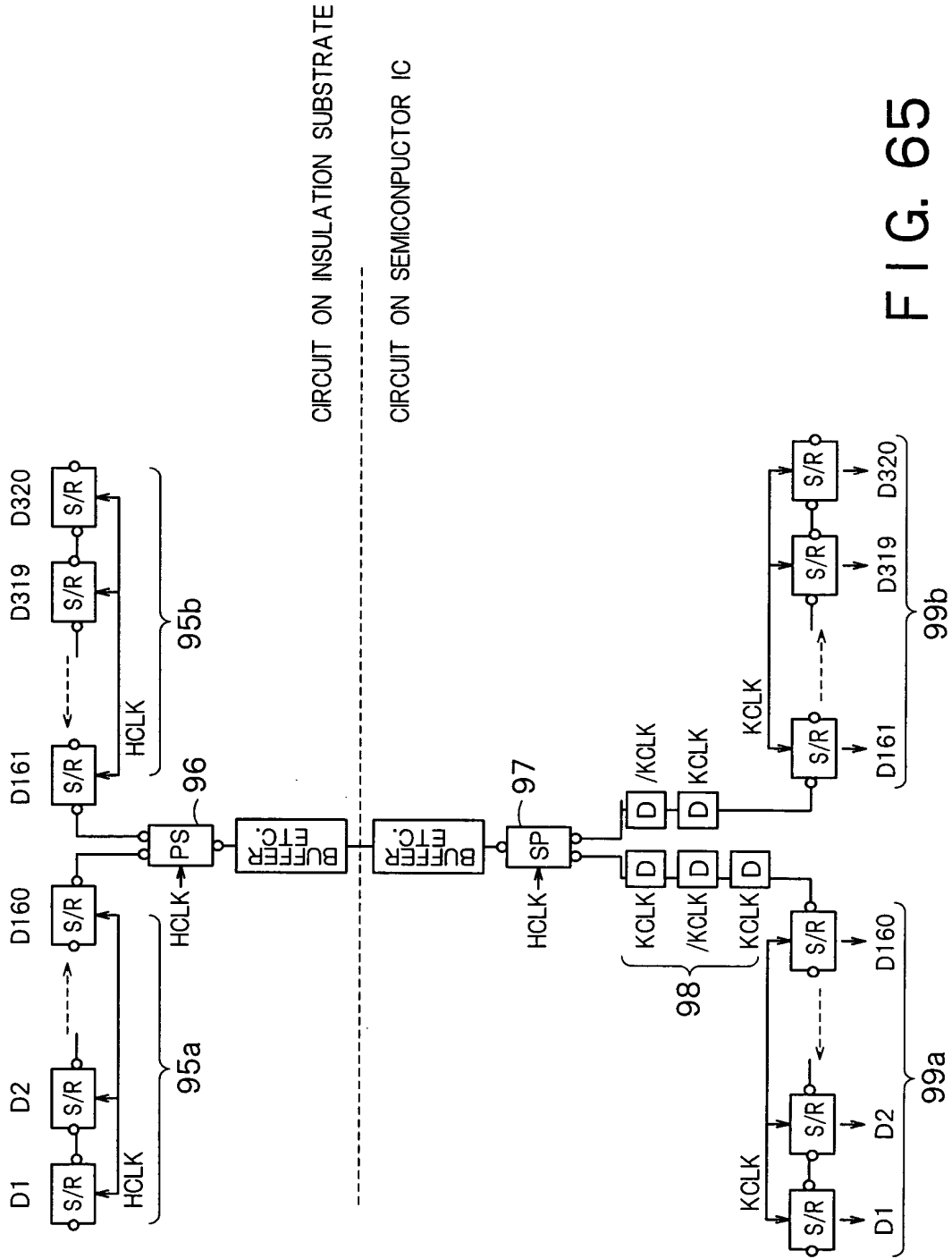


FIG. 65

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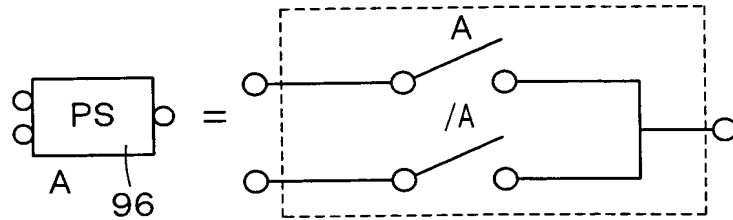


FIG. 66A

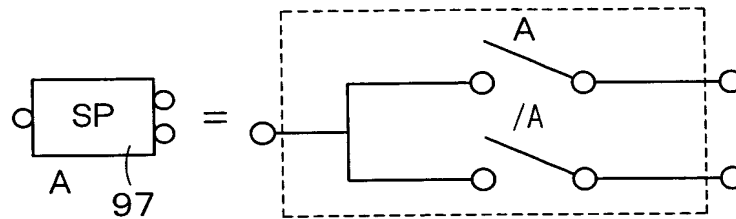


FIG. 66B

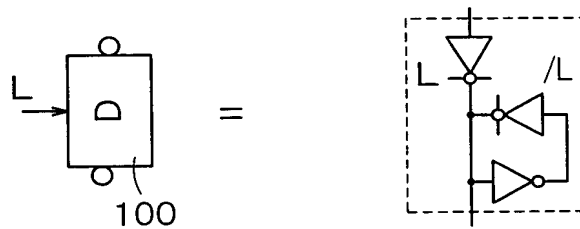


FIG. 67

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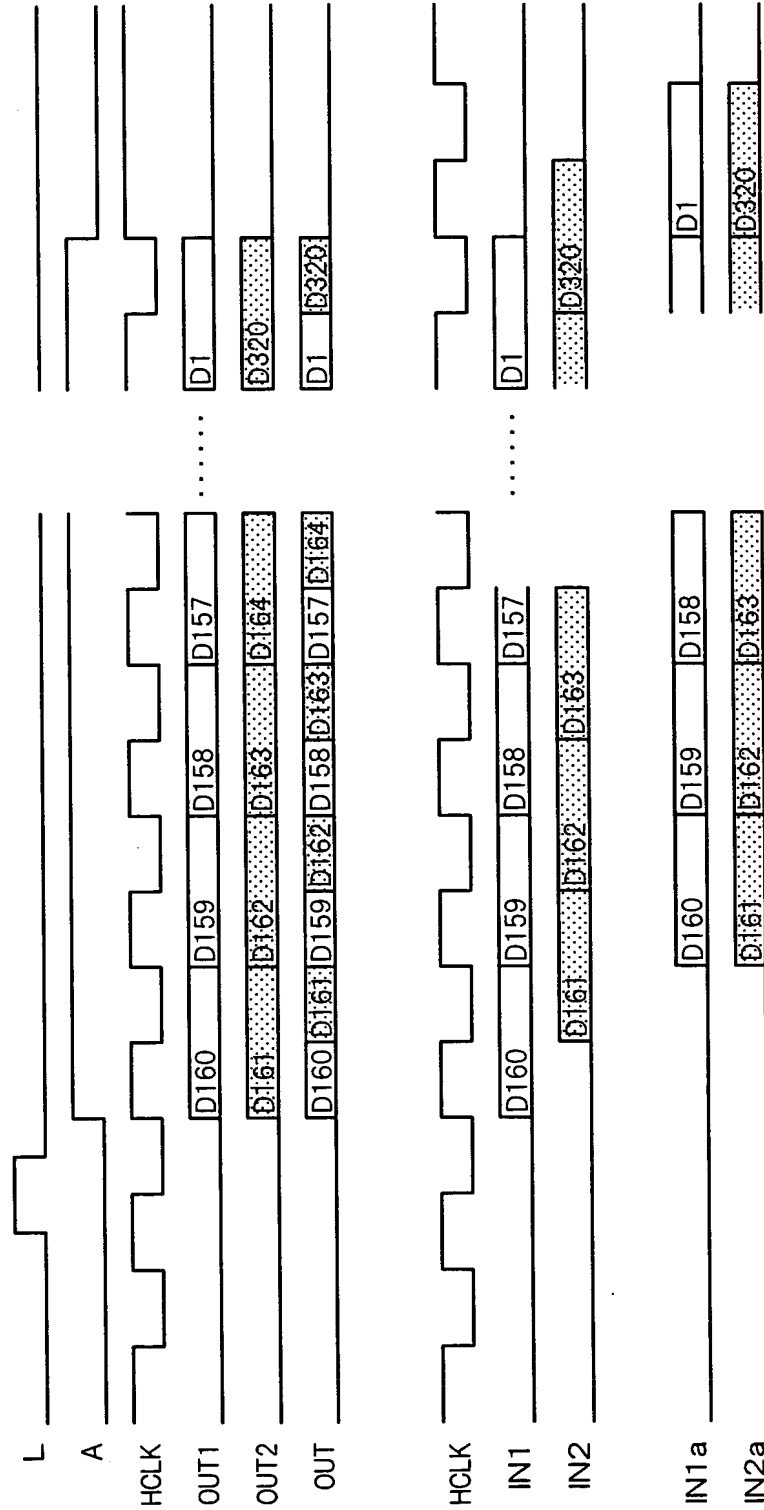


FIG. 68

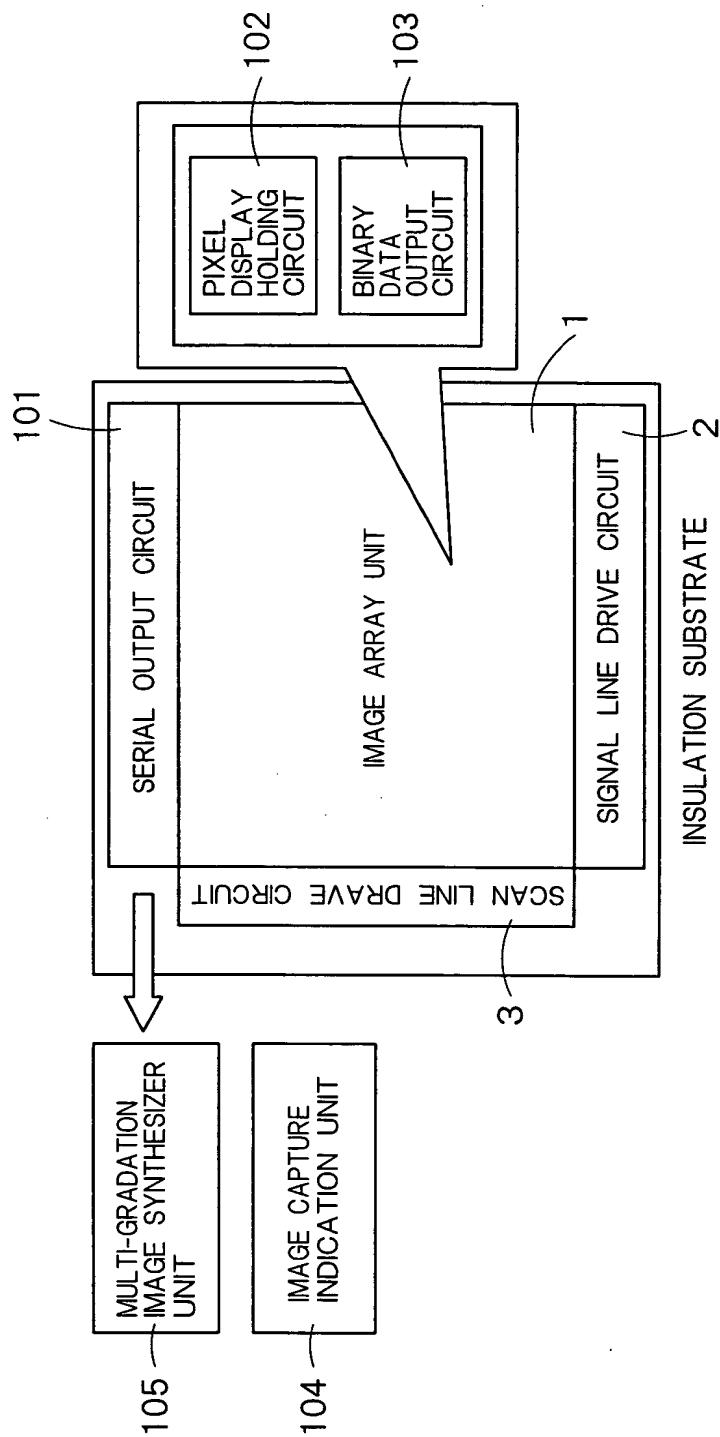


FIG. 69

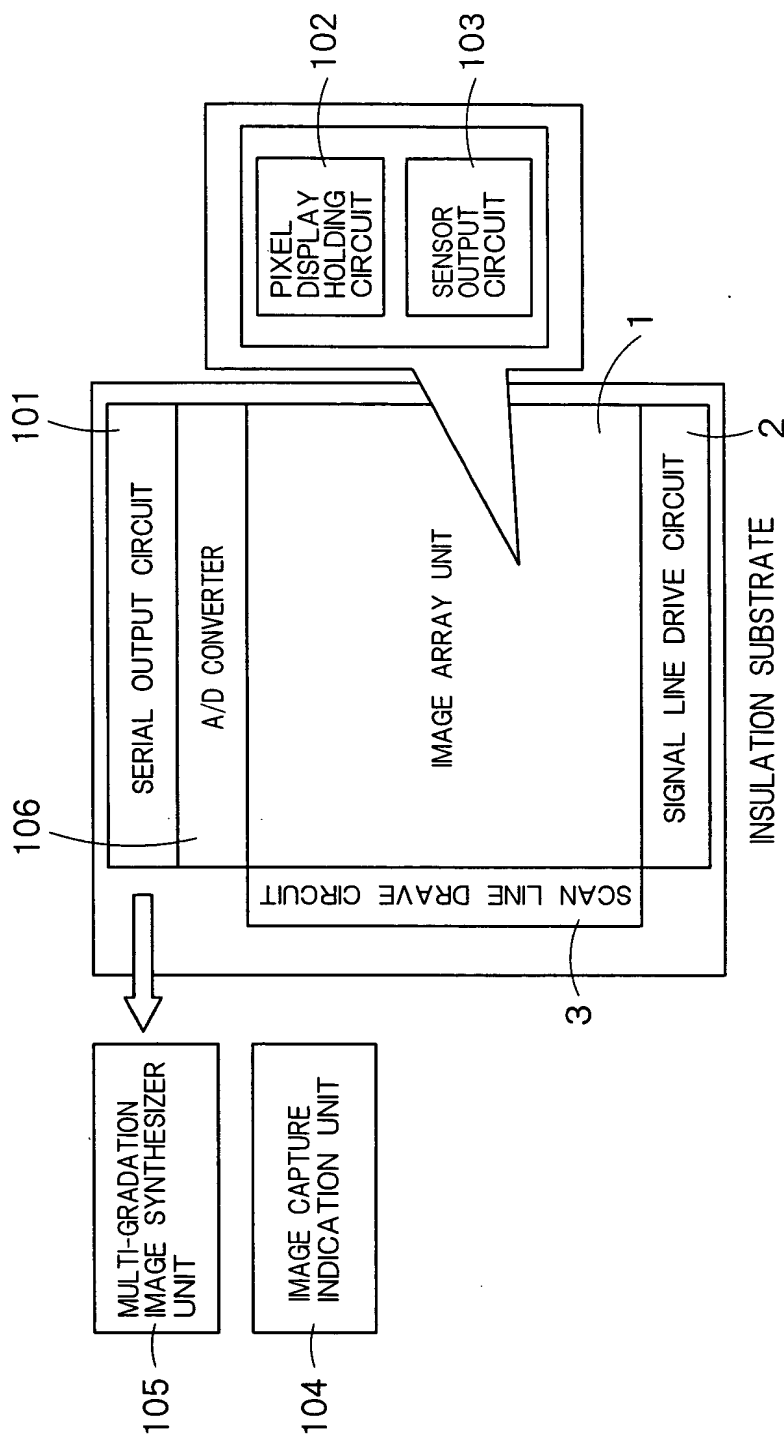


FIG. 70



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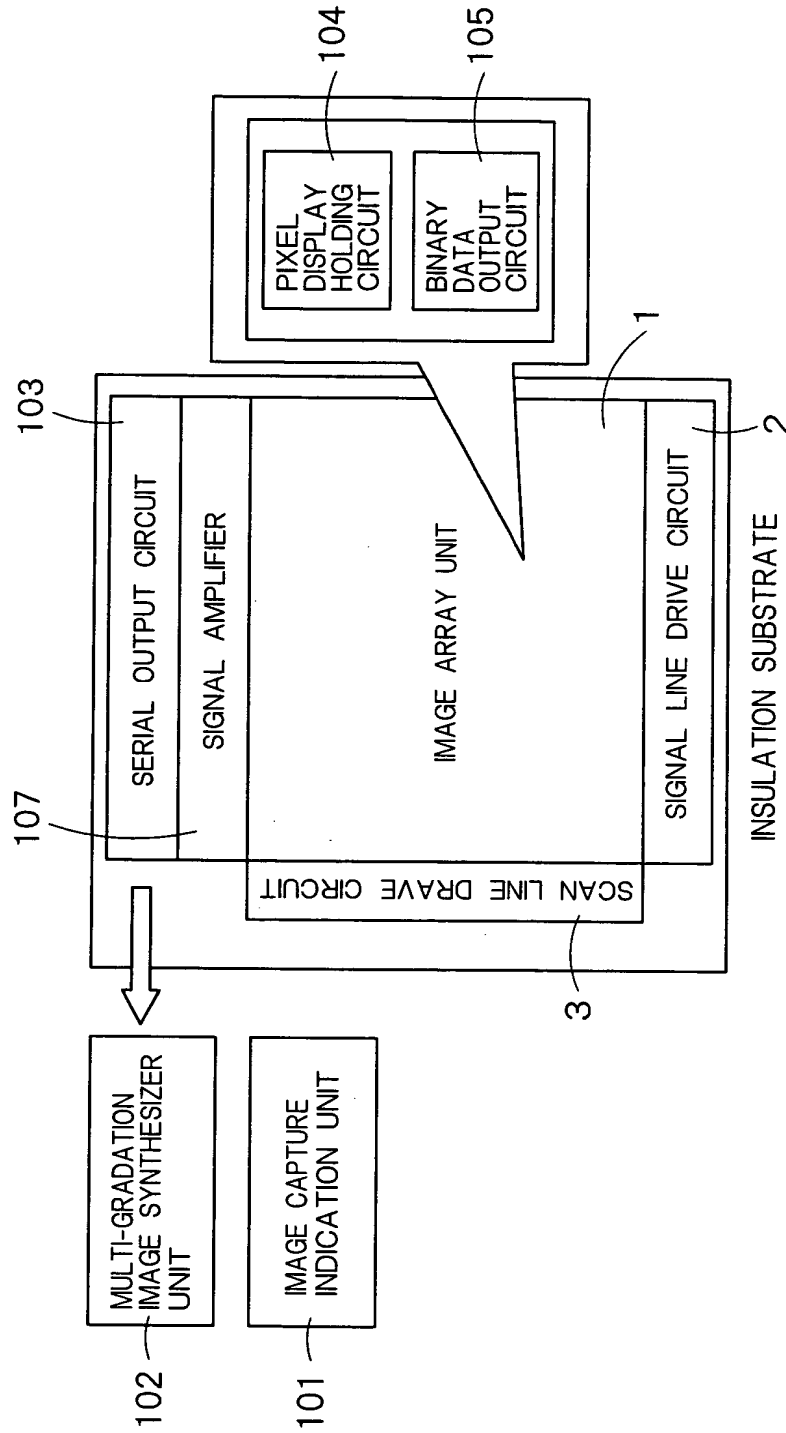


FIG. 71